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PURDUE UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING

A STUDY OF THE EXTENDED LINEAR RANGE PHASE LOCK LOOP

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John C. Lindenlaub
and
Donald P. Olsen

August 1968
Lafayette, Indiana

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ELECTRONIC SYSTEMS RESEARCH LABORATORY

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FOREWORD

This report is an interim report which summarizes one phase of research that is being carried out at Purdue University in the area of communication theory under NASA Grant NsG-553.

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ABSTRACT

A study was conducted to determine the performance of a phase lock loop with a linear modulo $2N\pi$ radian phase detector characteristic. Several of the limitations of the conventional phase lock loops are caused by the non-linear phase detector characteristic. Among these limitations the intermodulation distortion, the acquisition time and the threshold of the phase lock loop when used as an FM demodulator are the most critical. The first of these limitations is eliminated by using a linear phase detector with a range of $2N\pi$ radians. This research has been the investigation and analyzing of the effect of this phase detector upon the acquisition time and FM threshold.

The theoretical acquisition time for the high S/N case is determined, presented and compared with experimental data. The low S/N acquisition time is measured experimentally and a mathematical model based on regression analysis of this data is established.

The FM threshold is determined for a set of parameter values from experimental input/output S/N measurements. Both random and sinusoidal modulation are considered as well as first and second order systems. These are compared with the threshold of a standard phase lock loop demodulator.

It is concluded that two methods exist for exchanging low S/N threshold for improved high S/N threshold as well as increasing acquisition time. These are: 1. increasing the loop bandwith, 2. increasing the linear phase error range. The trade offs are equivalent for FM threshold in the cases considered, but increasing the loop bandwidth has a cubic improvement upon acquisition time and increasing the phase detector range only has a quadratic improvement upon the acquisition time. Therefore the optimum system when all three limitations are important is the phase lock loop with a linear 2π phase detector characteristic. The loop bandwidth is optimized to provide an acceptable level of limitation of the three performance criteria.

I. INTRODUCTION

1.1. Problem Statement

The Phase Lock Loop (PLL) has several limitations that are caused by the multiplier that is generally used for a phase detector. This phase detector has a sinusoidal phase characteristic when the inputs to it are sinusoids. The first limitation of interest is that this non-linearity within the loop generates intermodulation distortion (ID) in the loop's output when the loop is being used for FM demodulation. The greater the modulation index the greater the phase error and hence the greater the ID.

If the frequency of the signal to be demodulated is unknown then there will usually be an initial frequency error between that of the voltage controlled oscillator and that of the signal. In attempting to acquire lock, the loop phase error often exceeds $\pm \pi$ and causes a cycle slip to occur. This delays the acquisition process. For large frequency error to loop bandwidth ratios the acquisition time loop bandwidth product may be much greater than one. This is usually undesirable as faster acquisition means less information loss when used in a communication system.

Therefore it is desirable to increase the phase error range to something greater than $\pm \pi$. If the phase error range is increased to $\pm N\pi$, it is shown that the high signal to noise ratio (S/N) acquisition time is decreased and that for a given level of PLL output ID and modulation spectrum the maximum modulation index that can be demodulated is

increased over that of a PLL with sinusoidal phase detector phase characteristic.

However it is not obvious what effect this increase of the phase detector range has on the low S/N properties of a PLL. Therefore it is the purpose of this study to describe the low S/N continuous wave (CW) carrier acquisition and the FM threshold performance of a PLL with a linear modulo $2N\pi$ phase detector characteristic. N is a system parameter that is varied in the research. A linear characteristic over $2N\pi$ radians is considered since it yields the least ID for a given value of N.

1.2. Previous Work

The previous work on the PLL has been divided into primarily three areas: the PLL as an optimum demodulator, the optimization of the loop filter, and the effect of the phase detector non-linearity.

1.2.1. Optimum Demodulator

Youla [34] has derived a pair of integral equations which describes mathematically the maximum a posteriori (MAP) phase demodulator. For the infinite observation interval, they are

$$\theta(t) = - \int_{-\infty}^{\infty} R_{\phi}(t - u)\, A \,\mathrm{Sin}\, [\omega_c u + \theta(u)]\, g(u)\, du \qquad (1.1)$$

and

$$r(t) - A\, \mathrm{Cos}[\omega_c t + \theta(t)] = \int_{-\infty}^{\infty} R_n(t - u)\, g(u)\, du, \qquad (1.2)$$

where $r(t)$ is the received signal, $\phi(t)$ is the transmitted message in the form of phase modulation, $\theta(t)$ is the MAP estimate of $\phi(t)$, $R_{\phi}(\tau)$ is the autocorrelation function of $\phi(t)$, $R_n(\tau)$ is the autocorrelation function

of n(t), the additive gaussian noise in the channel, and where the transmitted signal is A $\text{Cos}[\omega_c t + \phi(t)]$.

Lindenlaub [12] has shown that the optimum demodulator equations can be interpreted in the form of a PLL with an unrealizable filter as shown in Figure 1.1 if

$$R_n(\tau) = N_0\delta(\tau) \tag{1.3}$$

and the bandwidth of $\phi(t)$ is much less than ω_c.

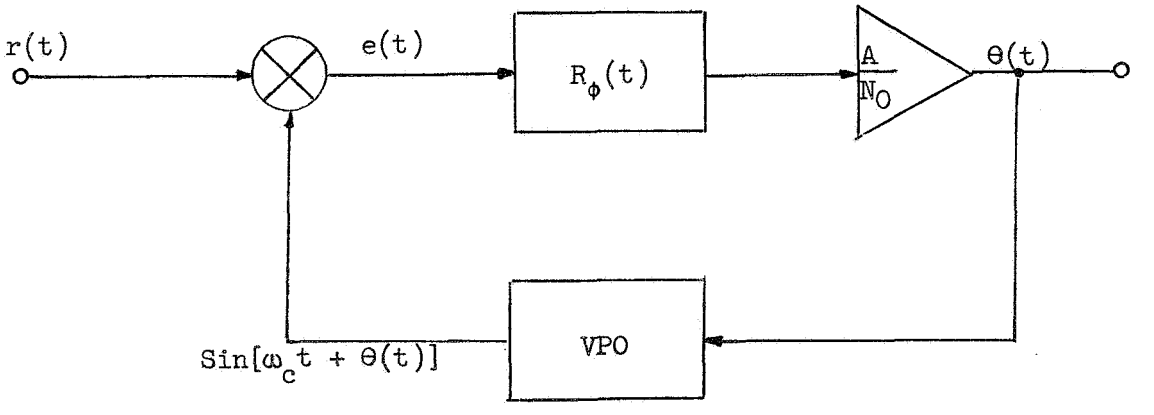

Figure 1.1. Optimum Demodulator as a PLL

To make this PLL realizable it is necessary to replace the unrealizable filter with a realizable one and add a post loop filter that will be unrealizable. However it is only possible to make the two systems equivalent at high S/N levels because of the multiplier in the loop. It is not clear that the realizable version of Figure 1.1 is the optimum realizable FM demodulator for low S/N levels. Therefore it is felt that the threshold behavior of the PLL as a frequency demodulator using various phase detector characteristics should be investigated both theoretically and

experimentally to see if an improvement in the degree of optimality of the PLL can be obtained.

1.2.2. Phase Lock Loop

The PLL is a popular though not a unique interpretation of the optimum frequency demodulator. Most of the references in the bibliography deal with the PLL. A more general version of the PLL will be considered here. Several authors [3, 5, 16, 17, 27, 33] consider non-linearities for the PLL phase detector other than the multiplier that appears in the MAP demodulator structure. Figure 1.2 is a block diagram of a generalized PLL.

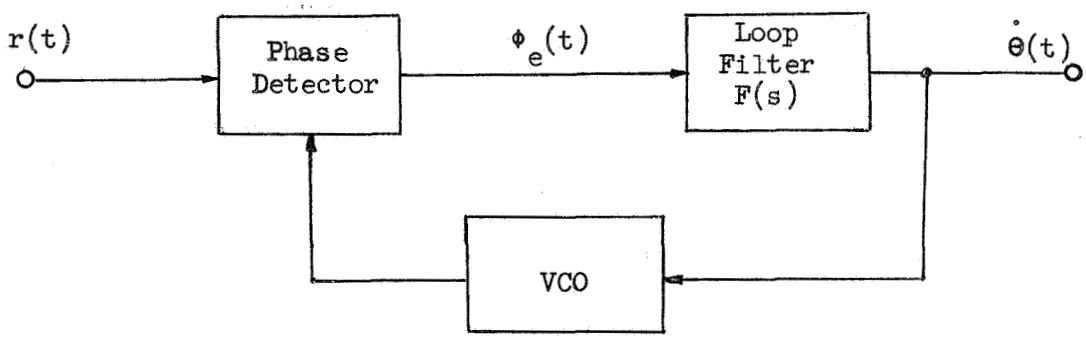

Figure 1.2. Generalized Phase Lock Loop

In the above system the phase of the incoming signal is compared with that of the voltage controlled oscillator (VCO) signal in the phase detector. In general the output of the phase detector, $\phi_e(t)$, is some function of the difference of the two phases. That is

$$\phi_e(t) = G[\phi(t) - \theta(t) + \psi(t)] \qquad (1.4)$$

where $\psi(t)$ is the phase noise due to n(t), and G is the function

describing the phase transfer function or the phase detector characteristic.

The error signal is operated on by the Loop Filter F(s). F(s) is usually designed so that the PLL will respond to a class of input signals and noise in some optimum way. Jaffe and Rechtin [11] derive the optimum F(s) for an input having gaussian noise plus step, ramp or quadratic time variation of signal phase. Their criteria of optimality is the minimization of the VCO output noise variance plus integral square transient error. Gilchriest [9] derives the optimum F(s) for FSK signals with gaussian noise. Both authors used a calculus of variations approach to determine the optimum physically realizable F(s).

In usual practice F(s) is a linear physically realizable filter with the form

$$F(s) = \frac{\sum_{j=0}^{m} a_j s^j}{\sum_{j=0}^{k} b_i s^i} \quad . \tag{1.5}$$

For the second order loop this simplifies to

$$F(s) = \frac{a_0 + a_1 s}{b_0 + b_1 s} \quad , \tag{1.6}$$

which is a lead or lag filter. It is also called a proportional plus imperfect integral filter when $b_0 \ll b_1 s$. For $b_0 = 0$, it is called a proportional plus integral filter. If $a_1 = 0$, it is a first order low pass filter. These three cases are most common in the literature [3, 5, 6, 9, 10, 11, 13, 14, 18, 19, 20, 21, 22, 23, 25, 27, 29, 30, 33].

A few authors [10, 11, 16, 20] consider the third order PLL where

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2}{s^3} \quad . \tag{1.7}$$

This results in a loop that will follow a signal with quadratic phase shift such as would be received from a transmitter that is being physically accelerated.

The author [16] has investigated the fourth order PLL with loop filter

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3}{s^3} \quad . \tag{1.8}$$

This PLL was very difficult to synchronize to an input signal because of the four independent initial conditions but extending the phase error range greatly reduced this problem.

Jaffe and Rechtin [11] proposed that F(s) be made variable so that it can be adapted to varying signal and noise levels so as to preserve optimality.

The filter output drives the VCO. The VCO has an output

$$e_{VCO} = 2\mathrm{Cos}[\omega_v t + \theta(t)]. \tag{1.9}$$

That is, it generates a cosine wave with a phase angle equal to the integral of the input plus a linear phase component, $\omega_v t$. The VCO output is used as a reference for the phase detector.

1.2.3. PLL Phase Detector Non-linearities

Most authors have studied the PLL having a multiplier phase detector. When the input and VCO signals are sine waves the multiplier phase detector yields a sinusoidal phase characteristic. Viterbi [32] and

Tikhonov [26] have found an exact expression for the phase error variance and probability density function (PDF) as well as the expected rate of cycle slipping for the first order loop having a multiplier. Only approximate results are available for the higher order PLL with a multiplier [6, 7, 13, 25, 30].

Byrne [3] was the first to investigate the use of another type of non-linearity. He was interested in the sawtooth phase detector characteristic and gives information on maximizing the capture range of the second order PLL. He provides many useful design curves as a function of the damping factor and the bandwidth.

Splitt [24] suggests, without proof, that the noise threshold of a PLL with a sawtooth characteristic should be lower than that for the PLL with multiplier. He argues that increasing the linear phase error range to 2π will reduce the probability of cycle slipping which in turn should decrease the impulse noise at the output.

Williams [33] and Cleland [5] have also studied this type of PLL. They investigated its acquisition properties and found that it has a greater probability of synchronizing to a noise free incoming signal than a PLL with a sinusoidal characteristic. Until now no theoretical data has been available concerning the noise threshold behavior of this type of PLL.

The literature mentions three ways for implementing a linear modulo $2N\pi$ phase detector. Byrne [3] suggested the use of frequency dividers as is shown in Figure 1.3 to obtain a $2N\pi$ linear range phase detector. The flip-flop is in the "ones" state for a length of time proportional to the modulo $2N\pi$ phase difference between Θ and Φ and $N\pi$. If the cut-off frequency of $F(s)$ is sufficiently lower than ω_c/N, the pulse-width

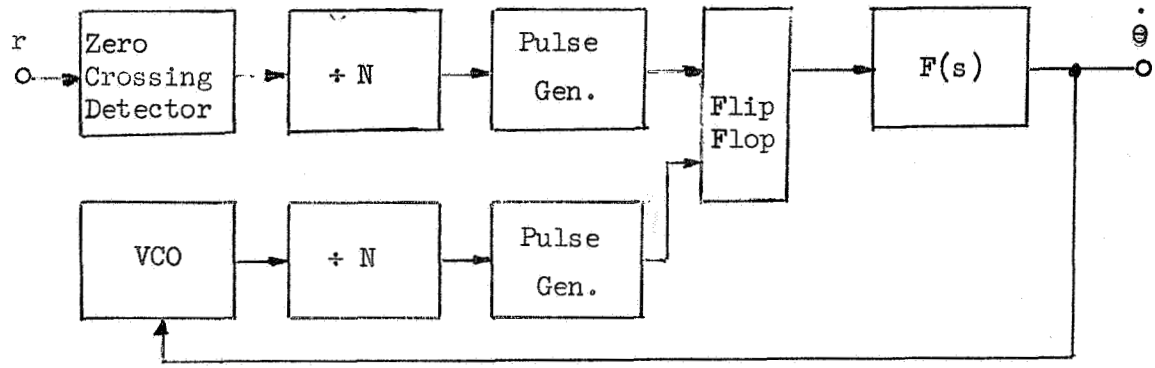

Figure 1.3. Byrne's Linear Modulo 2Nπ PLL

modulation of the flip-flop is converted to a DC level proportional to the average phase error. Here the size of N is limited by

$$\omega_c/B_m >> N \ , \tag{1.10}$$

where B_m is the maximum modulation frequency on the carrier. The cutoff frequency of F(s) must be much less than ω_c/N because the partially filtered rectangular phase detector output pulses would otherwise cause distortion of the VCO signal.

The author [16] used the system shown in Figure 1.4 to obtain a linear modulo 2Nπ phase detector characteristic to aid synchronization.

The author has shown [17] that an ideal discriminator followed by the non-linear filter as illustrated in Figure 1.5 is equivalent to a band-pass limiter (BPL) followed by a linear modulo 2Nπ PLL.

The sawtooth non-linearity has a period of 2Nπ radians. It is not yet clear how the BPL effects the threshold of any PLL. Reference [17] deals briefly with this question.

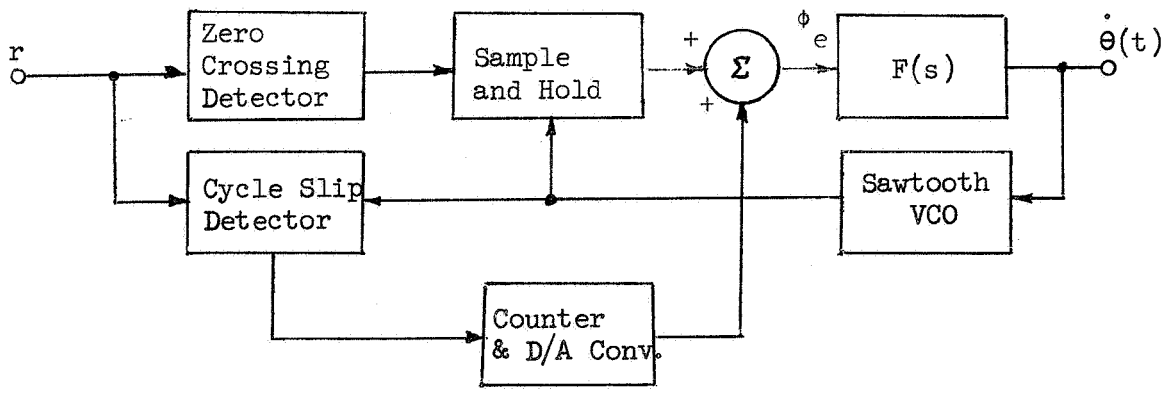

Figure 1.4. Linear Modulo 2Nπ Radian PLL System Used by the Author

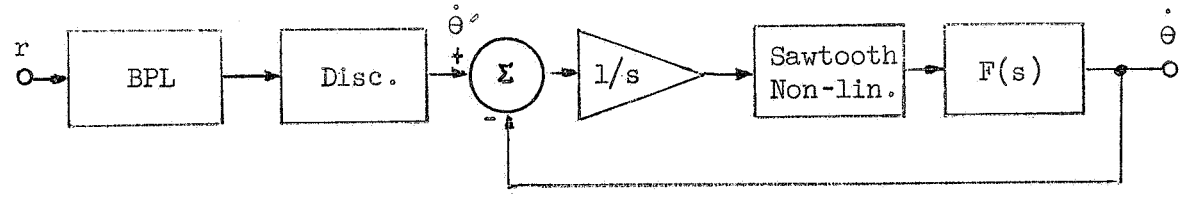

Figure 1.5. Equivalent Circuit for the 2Nπ Lin Lock Loop

Robinson [18] and Uhran [27] have studied the "Tan-lock" loop (TLL). The TLL has a phase detector with an output

$$e(t) = \frac{K_T r(t)\ \mathrm{Cos}[\omega_v t + \theta]}{1 + K_T r(t)\ \mathrm{Sin}[\omega_v t + \theta]}, \qquad (1.11)$$

where $\mathrm{Cos}[\omega_v t + \theta]$ and $\mathrm{Sin}[\omega_v t + \theta]$ are the VCO outputs and K_T the Tan-lock parameter, is such that $0 < K_T < 1$. If the S/N is high and the input envelope is 2, then the input signal can be approximated by

$$r(t) = 2\ \mathrm{Sin}[\omega_c t + \phi(t)]\,. \tag{1.12}$$

Neglecting double frequency terms

$$e(t) = \frac{K_T\ \mathrm{Sin}[\phi(t) - \theta(t)]}{1 + K_T\ \mathrm{Cos}[\phi(t) - \theta(t)]}\,. \tag{1.13}$$

As $K_T \rightarrow 1$

$$e(t) = \mathrm{Tan}\left[\frac{\phi(t) - \theta(t)}{2}\right]\,. \tag{1.14}$$

This is why the name "Tan-lock" has been given to PLLs having this phase detector.

Robinson [18] concludes that the lock range and acquisition probability of the TLL are much greater than those of a standard PLL. He also applied Boonton's technique [2] to predict the noise threshold behavior. He concluded that the TLL has a 2.4 to 4.4 db lower threshold when normalized to the high S/N loop bandwidth than the PLL with a sinusoidal phase detector characteristic.

Uhran [27] concluded from experimental results that the TLL has a higher threshold when normalized to the high S/N loop bandwidth than the PLL with sinusoidal phase detector characteristic. However, a normalization with respect to the lock range yielded the opposite conclusion.

This author believes that Robinson's conclusions are less correct then Uhran's since the former assumed a gaussian model for the VCO phase PDF. This assumption was shown to be inaccurate for the first order loop by Viterbi [32] and for the second order loop by Lindsey [13] for the low S/N case associated with the threshold region.

Acampora and Newton [1] propose that the phase range of the phase detector can be extended by including an internal "phase subtracting"

loop. For the case of a multiplier phase detector, this extends its linear phase range to greater than $\pi/2$. However they failed to consider that this internal loop could be absorbed into the linear loop filter by simply including a differentiator which results in a standard PLL as before with only a different linear loop filter.

Clark and Hess [4] propose two FM demodulator systems that are related to the PLL. Their systems are two implementations of "click" cancellation. They attempt to improve FM threshold by detecting the occurrence of clicks and claim an experimental threshold improvement over that of a conventional discriminator. They do not compare their results with those of the PLL. However their system is closely related to the PLL which this author built. (See Chapter VI) However there are two mathematical differences. The author's system does not have a multiplier after the phase detector and Clark and Hess' systems assume that N, the phase detector range constant, is infinite. Otherwise the author's system is mathematically equivalent to the two mentioned above.

Leon and Cleland [5] have investigated the properties of a PLL with a multiplier phase detector and a class of non-linear filters. They have been studying the acquisition properties of the first and second order loops. They have found optimum filters to improve the acquisition time. However they have not considered the performance of their systems at low S/N levels.

1.2.4. Analytical Techniques

Several mathematical techniques have been used to predict the phase error variance of PLLs. Develet [6] used Boonton's [2] technique to calculate an approximate "gain" for the phase detector but he also

assumed a gaussian PDF for the phase error. Therefore, the accuracy of his level for threshold is not known. This technique is valid for any phase error PDF but the distribution must be known to use it.

Tausworthe [25] used a spectral density approach and obtained curves for phase error variance that agree closely with the experimental results for the second order PLL, but he did not make any conclusions about threshold. This technique is valid for any type of additive noise that results in a phase error PDF that can be expressed as a diagonalized orthogonal expansion.

Margolis [14] used a series expansion for the phase detector and derived three terms. From these one can obtain an approximate expression for the phase error variance. He did not consider anything concerning the threshold.

Van Trees [30] used a Voltera expansion technique and by considering two terms was able to get an approximate expression for the phase error variance. He also did not conclude anything about the threshold. However, in another paper [29] he assumes that threshold occurs at a fixed phase error variance and obtains performance curves for output versus input S/N and modulation index based on a linear model for the PLL with the phase error variance as a constraint.

Viterbi [32] and Tikhonov [26] were able to obtain exact expressions for the phase error variance for the first order PLL with a sinusoidal characteristic using the Fokker-Planck equation but were unable to obtain tractable solutions for other cases. With this approach Lindsey [13] was able to obtain an approximate solution for the second order PLL with a sinusoidal non-linearity. From this, an approximate expression

for the phase error variance was obtained. However the significance of the remainder term in his result is uncertain.

Uhran [27] was unsuccessful in applying this technique to the Tan-lock PLL in a valid manner since Tan-lock has a division by a stochastic process.

1.2.5. Summary of the Limitations of Previous Work

The popular approach for comparing the degree of optimality of various systems has been to compare their phase error variance [6, 7, 14, 18, 25, 29, 30] or their output S/N [7, 16, 22, 23] or "threshold" level. The theoretical results have not been conclusive due to differences of definition [9, 22, 27]. Mathematical difficulties have prevented exact solutions except for the simplest cases [13, 26, 32]. Experimental results have not always been consistent from author to author [9, 22, 28]. This is perhaps due in part to incomplete definition of the experimental procedure. More often than not the approximate models used in theoretical work are not valid for the low S/N region where the threshold exists [6, 7, 25, 28]. This causes differences between the theoretical and experimental results.

Little work has been done on the low S/N performance of the PLL. This applies to both FM threshold, lock time and ID. Since there has been even less work on PLLs with non-sinusoidal phase detector non-linearities, it is not clear, for any of the three mentioned performance criteria, what type of non-linearity is best for the phase detector characteristic.

1.3. Areas of Research for This Work

Since the nature of the non-linearity in the phase detector of the realizable MAP demodulator is unknown and since increasing the linear range of the phase detector decreases both ID and acquisition time of a PLL, a study has been made of the FM threshold and low S/N acquisition time of a PLL with a linear modulo $2N\pi$ phase detector phase characteristic.

In Chapter III an analysis is made of the high S/N theoretical lock time of this type of PLL. This is done by programming a digital computer to calculate the piece wise continuous solution of the second order PLL differential equation. The lock time was calculated as a function of the initial phase error, frequency error and PLL damping ratio.

Chapter IV describes an experimental model of such a PLL and an additive noise channel as well as other test fixtures which were needed in the experimental work.

Chapter V describes an experiment that was devised and conducted to measure the acquisition time of the PLL for the set of loop and signal parameters. This set was designed so as to determine the effect of input S/N level, initial VCO frequency error, carrier frequency offset with respect to the center of the input noise spectrum, PLL damping ratio and the phase detector range constant N.

The theoretical and experimental results are presented in graphical form.

Chapter VI describes experiments that were devised and conducted to determine FM threshold by measuring the output S/N as a function of the input S/N for a set of PLL and signal parameters. This set was designed

to determine the effects of PLL damping ratio, PLL order, N, the input signal modulation spectrum, and FM index on the FM threshold phenomenon. The experimental results are presented in graphical form.

Chapter VII presents conclusions derived from this study and suggestions for further study are given.

1.3.1. Summary of New Results

The first area of interest in the acquisition time of the linear modulo $2N\pi$ PLL. It is shown that the theoretical decrease of the acquisition time of a second order linear modulo $2N\pi$ PLL for the high S/N case is

$$T_a = T_s \cdot .149/N \qquad (1.15)$$

where T_a and T_s are the acquisition times of the linear modulo $2N\pi$ PLL and sinusoidal PLL respectively. Experimental data agrees closely with this theoretical result. For most cases the low S/N acquisition time is an increasing function of the N/S ratio. But the rate of increase depends on the PLL damping, N, signal frequency offset from the center of the input noise spectrum, and initial VCO frequency error in a very involved manner. Regression analysis is used to determine an approximate model for this dependence.

The second area of interest is the FM threshold. Experimental data is presented. The conclusion of this study is that for a sufficiently high input S/N level the linear modulo $2N\pi$ PLL yields a lower threshold level than the sinusoidal PLL. The critical level appears to be about 20 db for sinusoidal and random modulation for a modulation bandwidth to PLL bandwidth ratio of .133. It is also determined that a decrease in the modulation bandwidth to PLL bandwidth ratio produces the same effect as an increase of N.

II. THEORY AND DEFINITIONS

The basic theory of the PLL used in this research is outlined in this chapter. The terms used that are peculiar to the PLL are also defined.

Figure 2.1 is a block diagram of a PLL with a generalized phase detector and a post loop low pass filter (LPF).

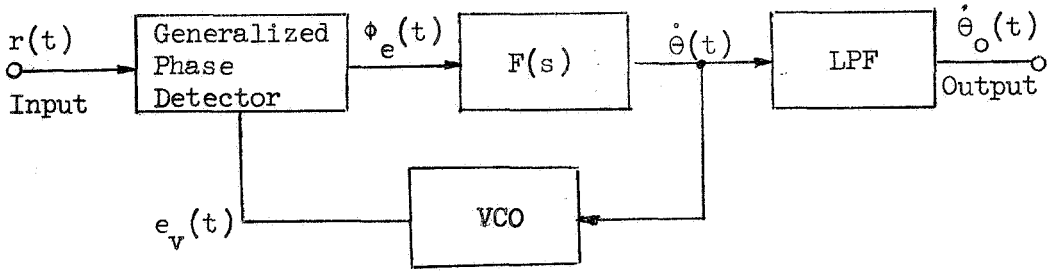

Figure 2.1. Generalized PLL with Post Loop Filter

In general the input r(t) consists of an FM sinusoid that has been corrupted by additive gaussian noise. The phase detector compares the phase of r(t) with that of the VCO output, $e_v(t)$, and produces an error signal, $\phi_e(t)$, that is a function, G, of the comparison. The loop filter operates upon this error signal and causes the VCO frequency to change in a direction to reduce the error. If there is no noise at the input and if the VCO is synchronized to the input signal frequency, the PLL is capable of determining the exact frequency of r(t). If the loop filter contains at least one additive ideal integrator the loop is able to estimate

exactly the phase of r(t). When noise is included in r(t), noise jitter appears in $\phi_e(t)$ and as the input noise is increased the accuracy of the estimate of the incoming frequency or phase is reduced.

If the frequency of r(t) is unknown it can be determined by the PLL. However the PLL must first be synchronized to r(t). Let the received signal be

$$r(t) = A \cos[\omega_c t + \phi] \tag{2.1}$$

and the VCO signal be

$$e_v(t) = 2 \cos[\omega_v t + \theta(t)]. \tag{2.2}$$

If it is assumed that G is linear for all ϕ_e, the synchronizing process is trivial. Then the loop is a linear system in the phase domain. The feedback of the system is such that for any value of initial frequency error the VCO frequency is continuously corrected by the loop so that eventually the frequency error is essentially zero. To demonstrate this let $F(s) = 1/T_1 s + K$, where s is the differential operator. Then clearly

$$\phi_e = \phi - \theta + (\omega_c - \omega_v)t \tag{2.3}$$

and

$$\theta = \phi_e \left(\frac{K}{s} + \frac{1}{T_1 s^2} \right) \tag{2.4}$$

or

$$\dot{\theta}(t) = \left[\omega_c - \omega_v \quad \dot{\phi}(t) \right] \frac{1 + KT_1 s}{1 + KT_1 s + T_1 s^2} \tag{2.5}$$

If $K > 0$, $T_1 > 0$, and $\phi(t)$ is constant

$$\lim_{t \to \infty} [\dot{\phi}(t) - \dot{\theta}(t) + \omega_c - \omega_v] = 0 \tag{2.6}$$

and

$$\lim_{t \to \infty} [\phi(t) - \theta(t) + (\omega_c - \omega_v)t] = 0. \tag{2.7}$$

However if G is not linear, these do not necessarily hold. Viterbi [31]

has shown that for sinusoidal G (2.6) and (2.7) are true. In Chapter III, (2.6) and (2.7) are shown to be true for the case of a linear modulo $2N\pi$ radian characteristic. This characteristic is given by

$$G[\phi - \theta + (\omega_c - \omega_v)t] = [\phi - \theta + (\omega_c - \omega_v)t + N\pi]_{\text{Mod } 2N\pi} - N\pi \qquad (2.8)$$

$$N = 1,2,\cdots .$$

Therefore this PLL will always acquire synchronization. In this study a PLL with a linear modulo $2N\pi$ radian phase detector is called the extended linear range PLL or ELRPLL. The time required for a PLL to synchronize is called the "lock time" or "acquisition time." Throughout this study the term acquisition time, T_a, is used and it is defined for the CW input signal plus additive gaussian noise case by the intersection of the following events

$$|\dot{\phi} - \dot{\theta} + \omega_c - \omega_v| < \frac{B_L}{2} \quad , \qquad (2.9)$$

$$\dot{\phi}_e(t)\ \dot{\phi}_e|_{t=0} < 0 \quad , \qquad (2.10)$$

and

$$|\phi_e(t)| < N\pi/10 \qquad (2.11)$$

where B_L is the PLL bandwidth.

If the initial frequency error is sufficiently large, the transient phase error predicted by a linear G is larger in magnitude than $N\pi$. When this happens in the ELRPLL a "cycle slip" occurs. That is, the phase detector output signal experiences a discontinuity and if ϕ_e prior to this event was $N\pi$ then just after the event ϕ_e will be $-N\pi$. All practical phase detectors are periodic in some multiple of 2π radians and hence all PLLs will exhibit cycle slip phenomenon.

Cycle slips can also be generated by the noise in r(t). If the noise causes the phase of r(t) with respect to that of e_v to encircle the origin sufficiently fast so that ϕ_e exceeds the phase detector range, then the ELRPLL will not be able to follow the transient and the phase error will generate a cycle slip.

The PLL is also used as an FM demodulator. Here the loop attempts to continually adjust the VCO frequency so that it follows the frequency variations of r(t). The VCO input signal under this condition is an estimate of the modulation. When r(t) contains additive noise, it is usually desirable to improve the S/N level of the demodulator output by filtering it with a post loop filter. The nature of the filter is usually low pass and the transfer function is often based on some optimizing criteria such as maximizing its output S/N level.

Throughout this study the loop bandwidth is understood to be the equivalent linear two sided noise bandwidth defined as follows

$$B_L = \frac{1}{2\pi} \int_{-\infty}^{\infty} d\omega \, H(j\omega) \, H^*(j\omega) \, , \tag{2.12}$$

where

$$H(s) = \frac{1 + KT_1 s}{1 + KT_1 s + T_1 s^2} \, . \tag{2.13}$$

For the first order ELRPLL, $T_1 = \infty$, and

$$H(s) = \frac{K}{K + s} \, . \tag{2.14}$$

In this case [15]

$$B_L = K/2 \, . \tag{2.15}$$

For the second order loop with finite non-zero T_1 [15]

$$B_L = (1 + K^2 T_1)/2KT_1 . \tag{2.16}$$

H(s) is called the closed loop transfer function.

It is desirable to minimize the frequency and intermodulation distortion in the demodulation output. Both can be reduced by increasing the loop bandwidth and the latter by increasing the phase detector's linear range. Increasing the loop bandwidth decreases the phase error and increasing the linear range of the phase detector reduces the distortion caused by it.

The word threshold is a term that is widely used to describe a poorly understood phenomenon. It is generally used in connection with FM demodulation as the name for the level of input S/N below which the demodulator ceases to function in some prescribed manner. In connection with the standard discriminator it is that level of input S/N where the output S/N "begins" to depart from a linear dependence upon the input S/N level. However this definition suffers because of its imprecise nature.

A popular definition for threshold used in connection with the PLL FM demodulator is a fixed level of phase error variance. This is usually set arbitrarily at .1 to .5 radians^2. However this is not a very satisfactory definition from a practical standpoint since the phase error here is defined as $\Phi - \Theta$ and this variable only exists in the mathematical model derived from the PLL. Note that Φ_e in the low S/N case for $f_c = f_v$ is not the same as $\Phi - \Theta$.

Gilchriest [9] used a novel definition. He defines threshold for FSK demodulation by a PLL as the level of input S/N for which the average signal suppression at the VCO input is 1%.

In the experimental work of Chapter VI, threshold is defined to be

the minimum input S/N level (referred to the output band) for which there exists a value of the modulation index for a given output S/N level. The appropriateness of this definition appears when one considers a typical input/output S/N plot of an FM demodulator for a class of modulation indexes. In general this family of curves defines the boundary of a forbidden region similar to that which Develet [6] gives in Figure 4 for the PLL threshold and Shannon's limit.

III. THEORETICAL ELRPLL ACQUISITION TIME

Chapter III presents a theoretical analysis of the acquisition time of the ELRPLL. This is done for the case of no modulation and high S/N level for a second order loop. It is assumed that the loop filter is

$$F(s) = K + 1/T_1 s. \tag{3.1}$$

It is assumed that at t = 0, there is some known initial frequency error $\Delta f(0)$, and some known initial phase error $\phi_e(0)$. The acquisition time is found as a function of B_L, the loop damping (ξ), the phase error range constant (N), the initial frequency error and initial phase error. The results are presented in graphical form and are compared with Viterbi's result [31] for a PLL with a sinusoidal phase detector.

3.1. Mathematical Model

The phase detector characteristic of the ELRPLL is

$$G(\phi_B) = (\phi_B + N\pi)\Big|_{\text{Mod } 2N\pi} - N\pi \ , \tag{3.2}$$

where

$$\phi_B = \phi - \theta + (\omega_c - \omega_v)t. \tag{3.3}$$

Then recalling from Figure 2.1 that θ is related to ϕ_B by F(s)/s one can show that

$$T_1 \frac{d^2\phi_B}{dt^2} + KT_1 \frac{d\phi_e}{dt} + \phi_e = 0 \tag{3.4}$$

together with equation (3.2) define the ELRPLL system. Except for the

points $\phi_B = MN\pi$, $M = \pm 1, \pm 3, \cdots$, the system is linear and the solution is trivial. Under this condition it is meaningful to speak of the system bandwidth, B_L, and damping ratio, ξ.

It is advantageous to redefine the system equations in terms of B_L and ξ.

Let the normalized time be

$$\tau = B_L t. \tag{3.5}$$

Note that the damping ratio is

$$\xi = .5KT_1^{.5}. \tag{3.6}$$

Let the phases ϕ_B and ϕ_e be normalized by letting

$$\phi_e' = \phi_e / N \tag{3.7}$$

and

$$\phi_B' = \phi_B / N . \tag{3.8}$$

Then the ELRPLL is defined by

$$\phi_e' = (\phi_B' + \pi)_{\text{Mod } 2\pi} - \pi \tag{3.9}$$

and

$$a^2 \frac{d^2\phi_B'}{d\tau^2} + 2\xi a \frac{d\phi_e'}{d\tau} + \phi_e' = 0, \tag{3.10}$$

where

$$a = \frac{1 + 4\xi^2}{4\xi}. \tag{3.11}$$

3.2. Underdamped Case

The solution for $\xi < 1$ is

$$\phi_B'(\tau) = \text{Exp}\ (-\alpha\tau)\ [A\ \text{Cos}(\omega_1\tau) + B\ \text{Sin}(\omega_1\tau)] \tag{3.12}$$

where

$$\alpha = \frac{4\xi}{a}, \tag{3.13}$$

$$\omega_1 = \frac{(1 - \xi^2)^{.5}}{a}, \tag{3.14}$$

$$B = \phi'_B(0) \tag{3.15}$$

and

$$A = \omega_1 \phi'_B(0) - \dot{\phi}'_B(0). \tag{3.16}$$

The normalized frequency error is given by

$$\Delta f'(\tau)/N = \frac{1}{2\pi} \dot{\phi}'_B(\tau) = \frac{1}{2\pi} \text{Exp}(-\alpha\tau)[(B\omega_1 - A\alpha)\,\text{Cos}(\omega_1\tau) - (A\omega_1 + B\alpha) \cdot \text{Sin}(\omega_1\tau)]. \tag{3.17}$$

Note that using (3.12) through (3.17) it is possible to choose $\Delta f'(0)$ and $\phi'_B(0)$ such that $|\phi'_B(\tau)| < \pi$ for all $\tau > 0$. However this is not true for all $\Delta f'(0)$ and $\phi'_B(0)$. When this is not true there is a set of $\tau_i > 0$, call them τ_i, $i = 1, 2, .., M$, for which $\phi'_e = \pi$. At these points ϕ'_e passes through a discontinuity. The boundary conditions at the discontinuity are

$$\dot{\phi}_e(\tau_i^+) = \dot{\phi}'_e(\tau_i^+) + \phi'_e(\tau_i^-)\frac{2\xi}{a} \tag{3.18}$$

and

$$\phi_B(\tau_i^+) = \phi_B(\tau_i^-) \tag{3.19}$$

for $i = 1, 2, \ldots, M$. Appendix A describes a digital computer program used to calculate ϕ'_e and $\Delta f'$ for several values of τ, ξ, $\Delta f'(0)$ and $\phi'_e(0)$ from (3.12) through (3.19). From this calculation, $T'_a(\Delta f')$ is plotted for several $\phi'_e(0)$ and $\xi = .25$ in Figure 3.1, $\xi = .35$ in Figure 3.2, $\xi = .5$ in Figure 3.3 and $\xi = .707$ in Figure 3.4.

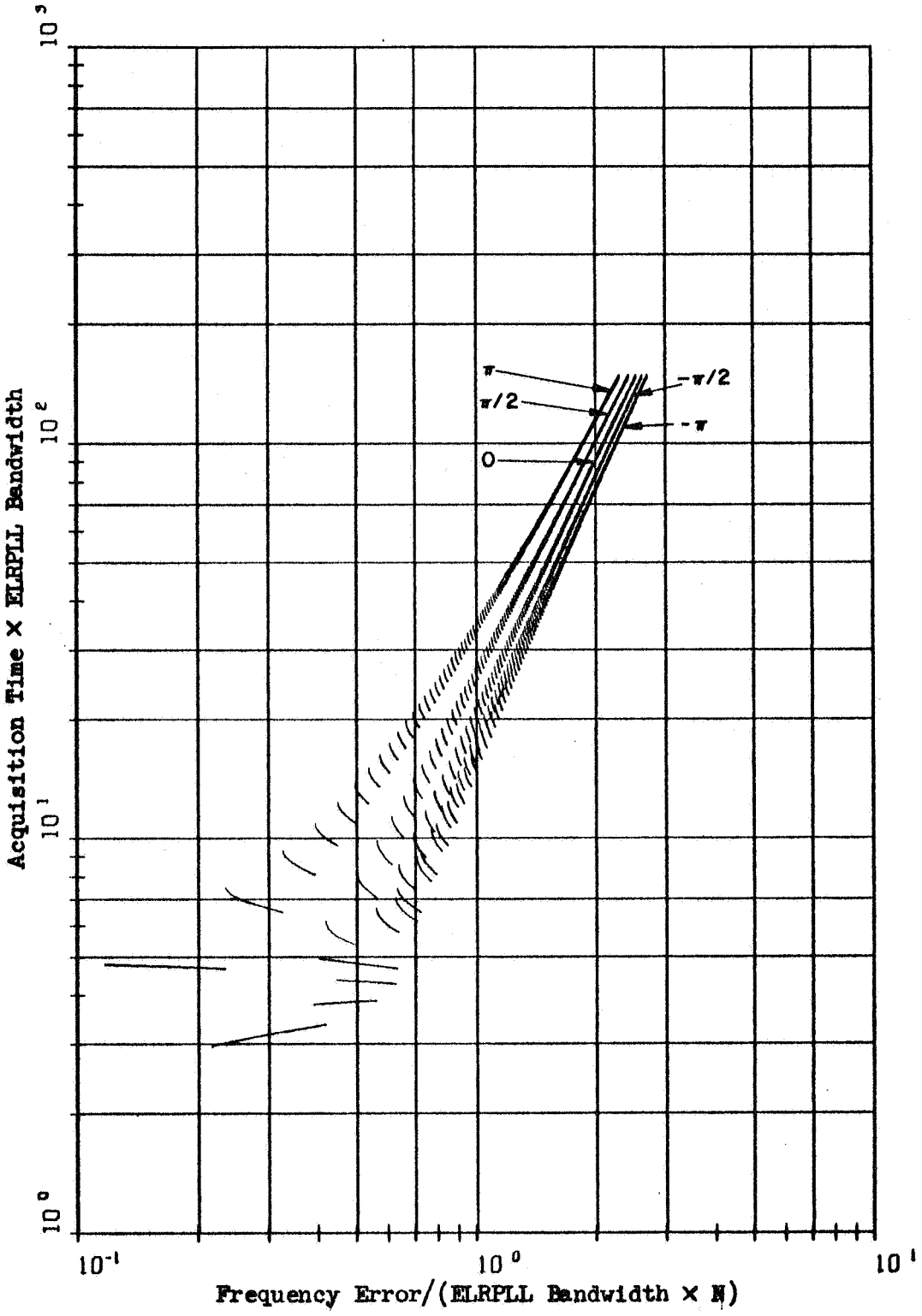

Figure 3.1. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to .25

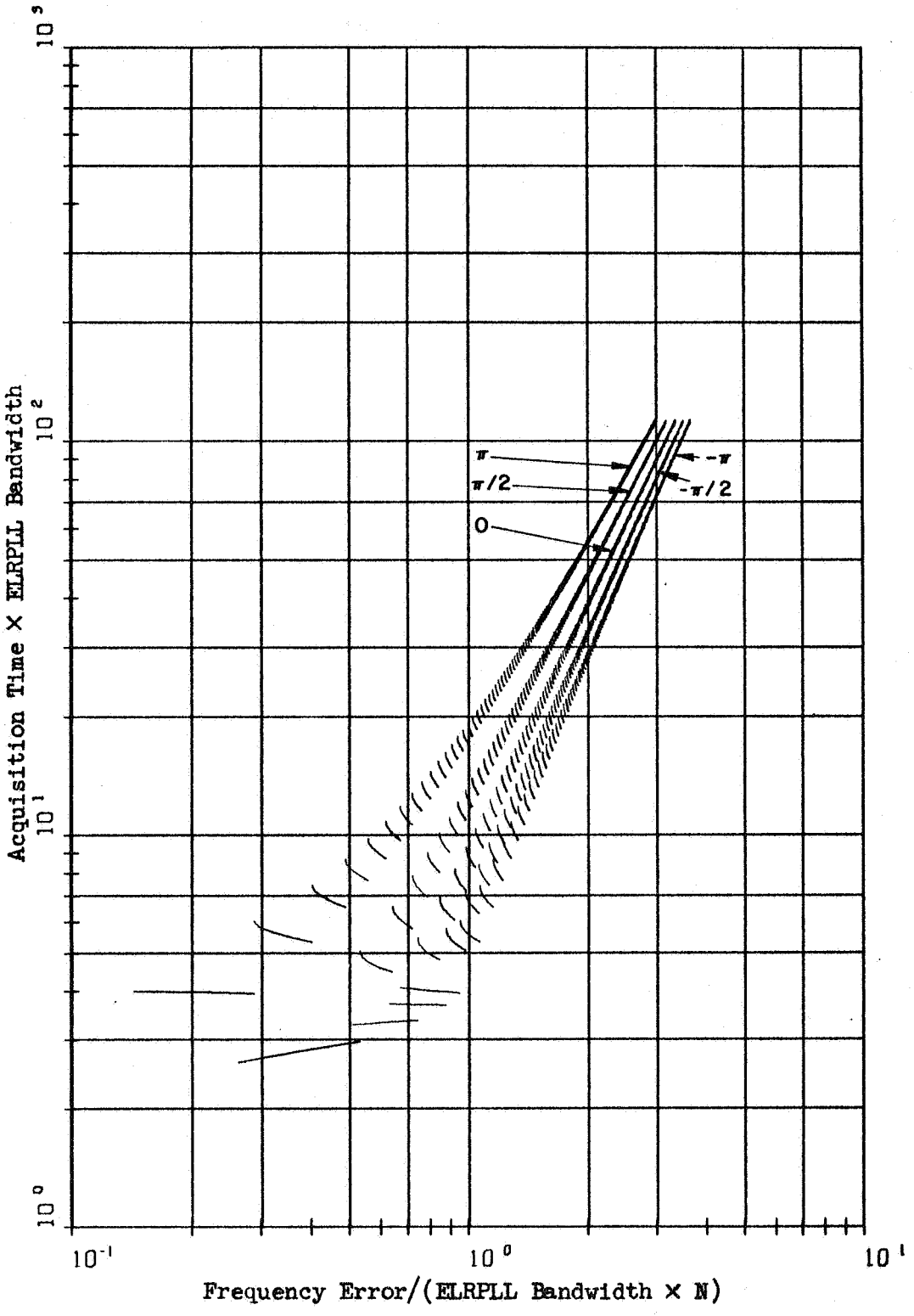

Figure 3.2. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to .35

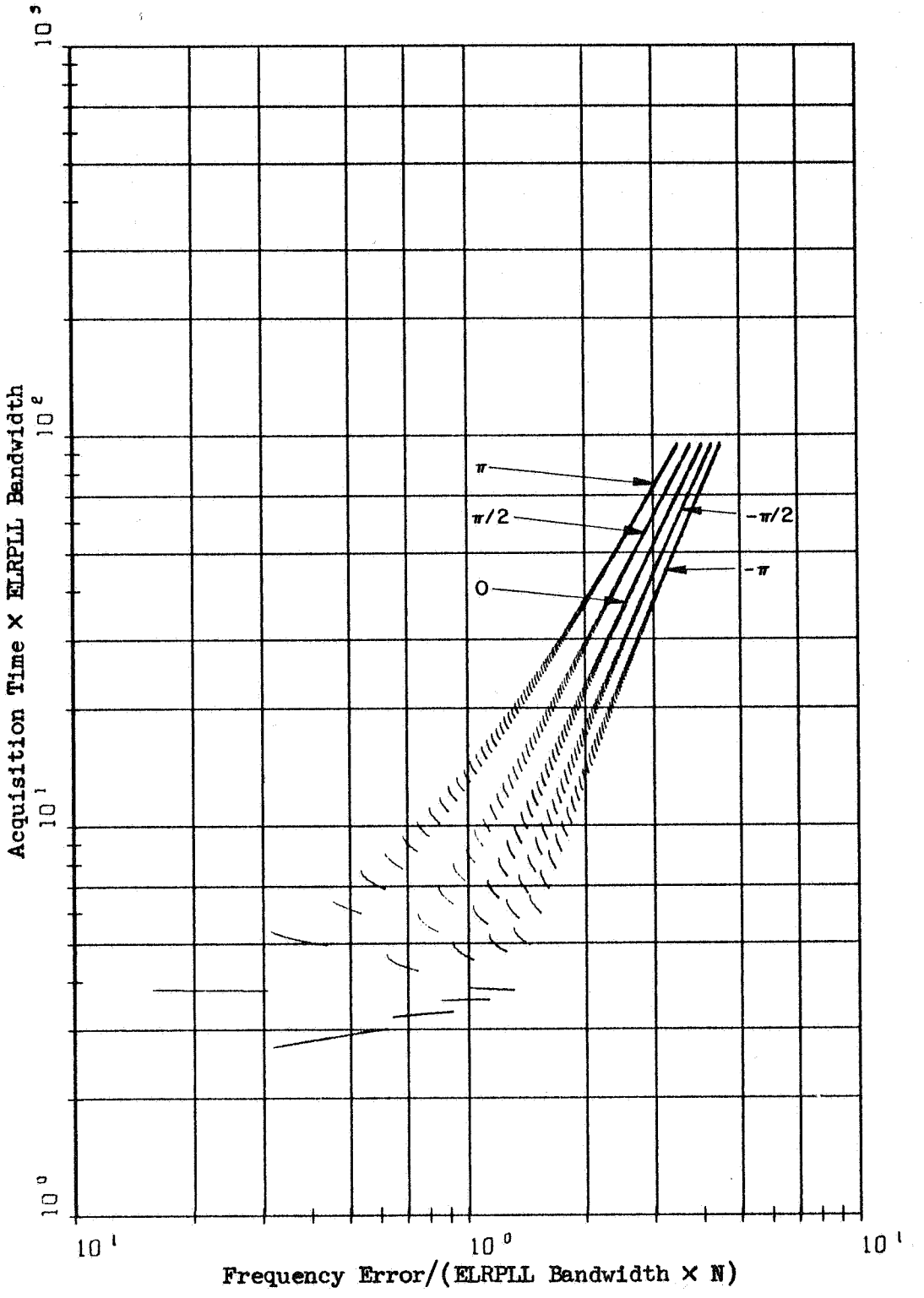

Figure 3.3. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to .5

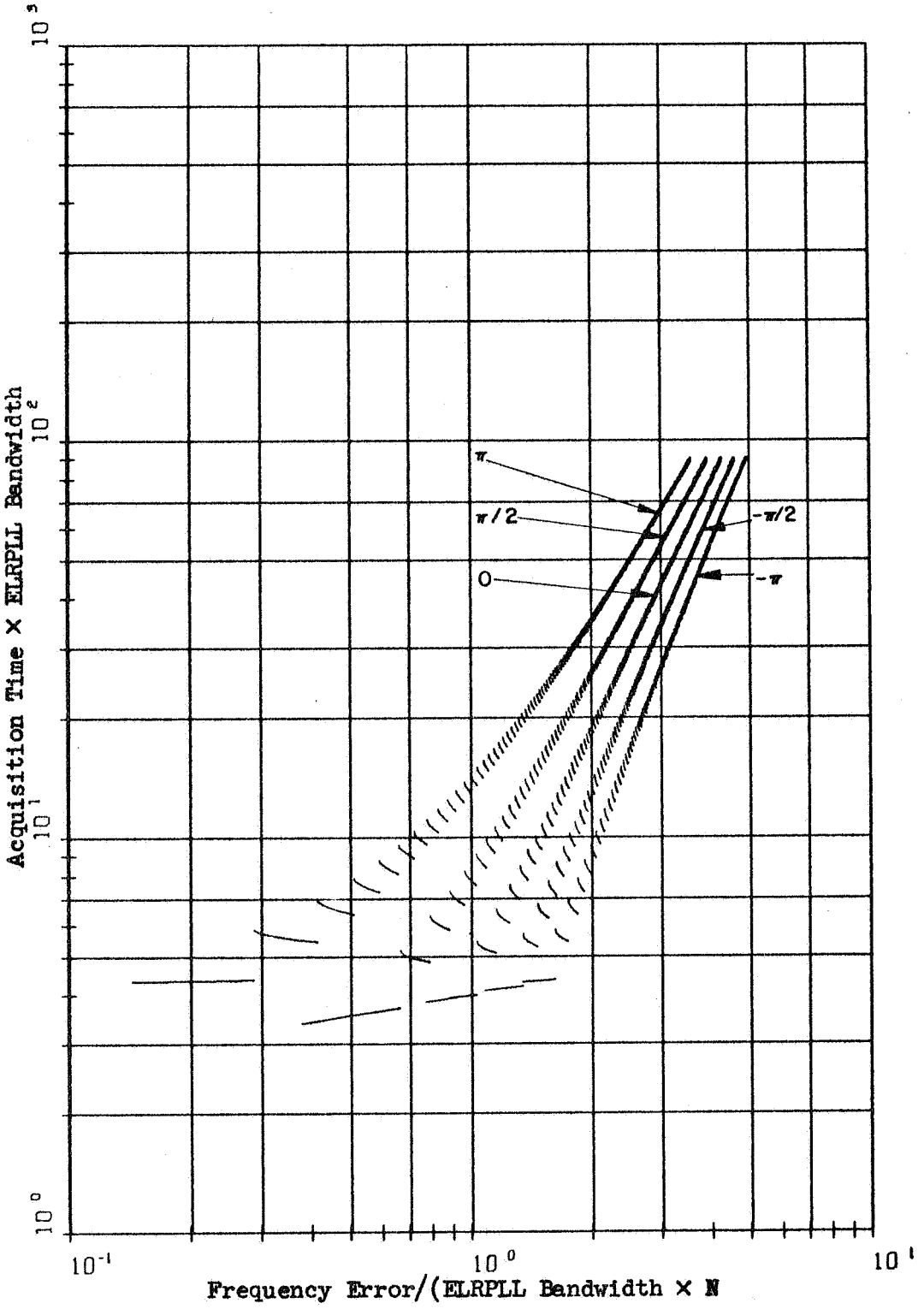

Figure 3.4. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to .71

3.3. Critically Damped Case

The solution of (3.10) for $\xi = 1$ is

$$\phi_B'(\tau) = (A + B\tau)\ \mathrm{Exp}(-\alpha\tau) \tag{3.20}$$

where

$$\alpha = \frac{16\xi^2}{1 + 4\xi^2}\ , \tag{3.21}$$

$$A = \phi_B'(0) \tag{3.22}$$

and

$$B = \alpha\phi_B'(0) + \dot{\phi}'(0)\ . \tag{3.23}$$

The normalized frequency error is given by

$$\Delta f'(\tau)/N = \frac{1}{2\pi}\ \dot{\phi}_B'(\tau) = \frac{1}{2\pi}\ [B - \alpha(A + B\tau)]\ \mathrm{Exp}(-\alpha\tau)]. \tag{3.24}$$

Note that using (3.20) through (3.24) it is possible to choose $\Delta f'(0)$ and $\phi_B'(0)$ such that $|\phi_B'(\tau)| < \pi$ for all $\tau > 0$. However just as in Section 3.2 this is not true in general. When it is not true there is a set of τ_i, $i = 1, \ldots, M$ for which $\phi_e' = \pi$. At these points ϕ_e' passes through a discontinuity. The boundary conditions at the discontinuity are the same as before.

$$\dot{\phi}_e'(\tau_i^+) = \dot{\phi}_e'(\tau_i^-) + \phi_e'(\tau_i^-)\ \frac{2\xi}{a} \tag{3.25}$$

and

$$\phi_B'(\tau_i^+) = \phi_B'(\tau_i^-) \tag{3.26}$$

for $i = 1, \ldots, M$. The digital computer program described in Appendix A was also used for this case to calculate ϕ_e' and $\Delta f'$ for several values of τ, $\Delta f'(0)$ and $\phi_e'(0)$ from (3.20) through (3.26). From this calculation, $T_a'(\Delta f')$ is plotted for several values of $\phi_e'(0)$ and $\xi = 1$ in Figure 3.5.

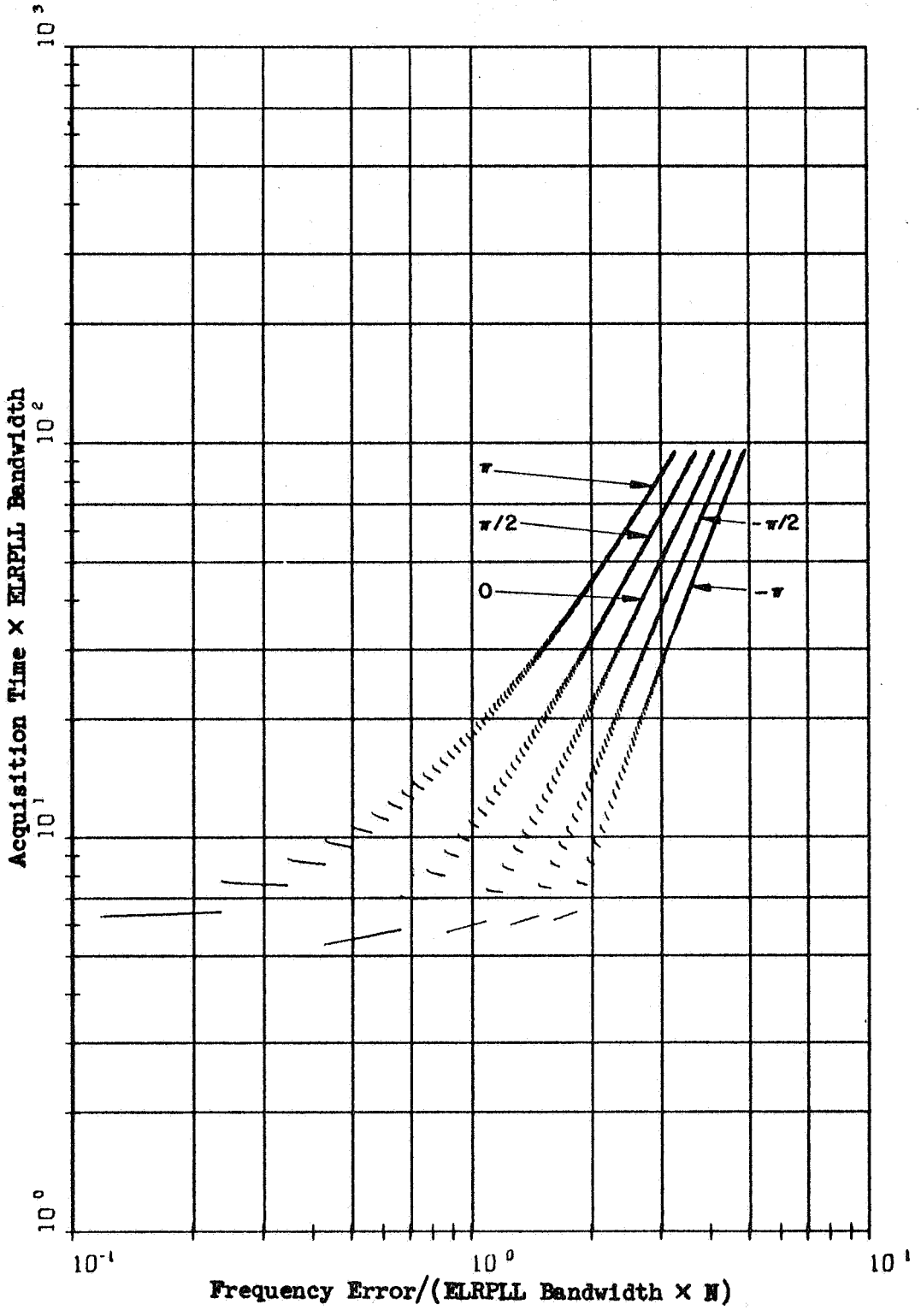

Figure 3.5. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to 1

3.4. Overdamped Case

The solution of (3.10) for $\xi > 1$ is

$$\phi_B'(\tau) = A \exp(- \alpha\tau) + B \exp(- \beta \tau) \tag{3.27}$$

where

$$\alpha = \frac{\xi + (\xi^2 - 1)^{.5}}{a}, \tag{3.28}$$

$$\beta = \frac{\xi - (\xi^2 - 1)^{.5}}{a}, \tag{3.29}$$

$$A = \frac{\dot{\phi}_B(0) + B\phi_B'(0)}{\beta - \alpha} \tag{3.30}$$

and

$$B = \frac{\dot{\phi}_B'(0) + \alpha\phi_B'(0)}{\alpha - \beta}. \tag{3.31}$$

The normalized frequency error is

$$\Delta f'(\tau)/N = \frac{1}{2\pi} \dot{\phi}_B'(\tau) = \frac{1}{2\pi} [A\alpha \exp(- \alpha\tau) + B\beta \exp(- \beta\tau)]. \tag{3.32}$$

Note that using (3.26) through (3.31) it is possible to choose $\Delta f'(0)$ and $\phi_B'(0)$ such that $|\phi_B'(\tau)| < \pi$ for all $\tau > 0$. However just as in sections 3.2 and 3.3 this is not true in general. When it is not true there is a set of τ_i, $i = 1, \ldots, M$ for which $\phi_e' = \pi$. At these points ϕ_e' passes through a discontinuity. The boundary conditions at the discontinuity are the same as before:

$$\dot{\phi}_e'(\tau_i^+) = \dot{\phi}_e'(\tau_i^-) + \phi_e'(\tau_i^-) \frac{2\xi}{a} \tag{3.33}$$

and

$$\phi_B'(\tau_i^+) = \phi_B'(\tau_i^-) \tag{3.34}$$

for $i = 1, \ldots, M$. The same digital computer program is also used to calculate ϕ_e' and $\Delta f'$ for several values of τ, ξ, $\Delta f'(0)$ and $\phi_e'(0)$ from (3.27)

through (3.34). From this calculation $T_a''(\Delta f'')$ is plotted for several values of $\phi_e''(0)$ and $\xi = 1.4$ in Figure 3.6 and for $\xi = 2.0$ in Figure 3.7.

Note that for each value of ξ the acquisition time for small $|\Delta f''|/N$, is greatly dependent upon the initial phase error and that for increasing $|\Delta f''|/N$ this dependence is a smaller proportion of the total acquisition time. However the amount of variation of $|\Delta f''|$ with ϕ_e'' for a given T_a'' is independent of T_a''.

Note that the scallops of the curves are caused by the cyclic nature of the phase detector characteristic and that the discontinuities are caused by the discontinuous nature of the phase detector. In general the continuous portions of the curves have negative slopes except for the first 1 or 2 scallops on some of the curves.

Note that increasing $\phi_e''(0)$ causes an increase of T_a'' for most cases of $|\Delta f''|/N$ and ξ. Increasing $\phi_e''(0)$ also increases $\dot{\phi}_e''$ at each cycle slip point and hence increases the number of cycle slips and also T_a''.

3.5. ELRPLL Transient Response to a Frequency Step

The transient phase error of the ELRPLL for a frequency step input is examined in this section. The peculiar nature of the acquisition time curves is better understood when one is familiar with the transient phase error of this system to a step in input frequency. The computer program described in Appendix A is used to plot $\phi_e''(\tau)$ for $\Delta f''(0)/N = 2$, $\phi_e''(0) = 0$ and various ξ in Figure 3.8. It is apparent that the discontinuities in the transient phase error correspond to those in Figures 3.1 through 3.7. Note that at the peak of each cycle of the transient phase error a discontinuity occurs unless the slope is zero at that

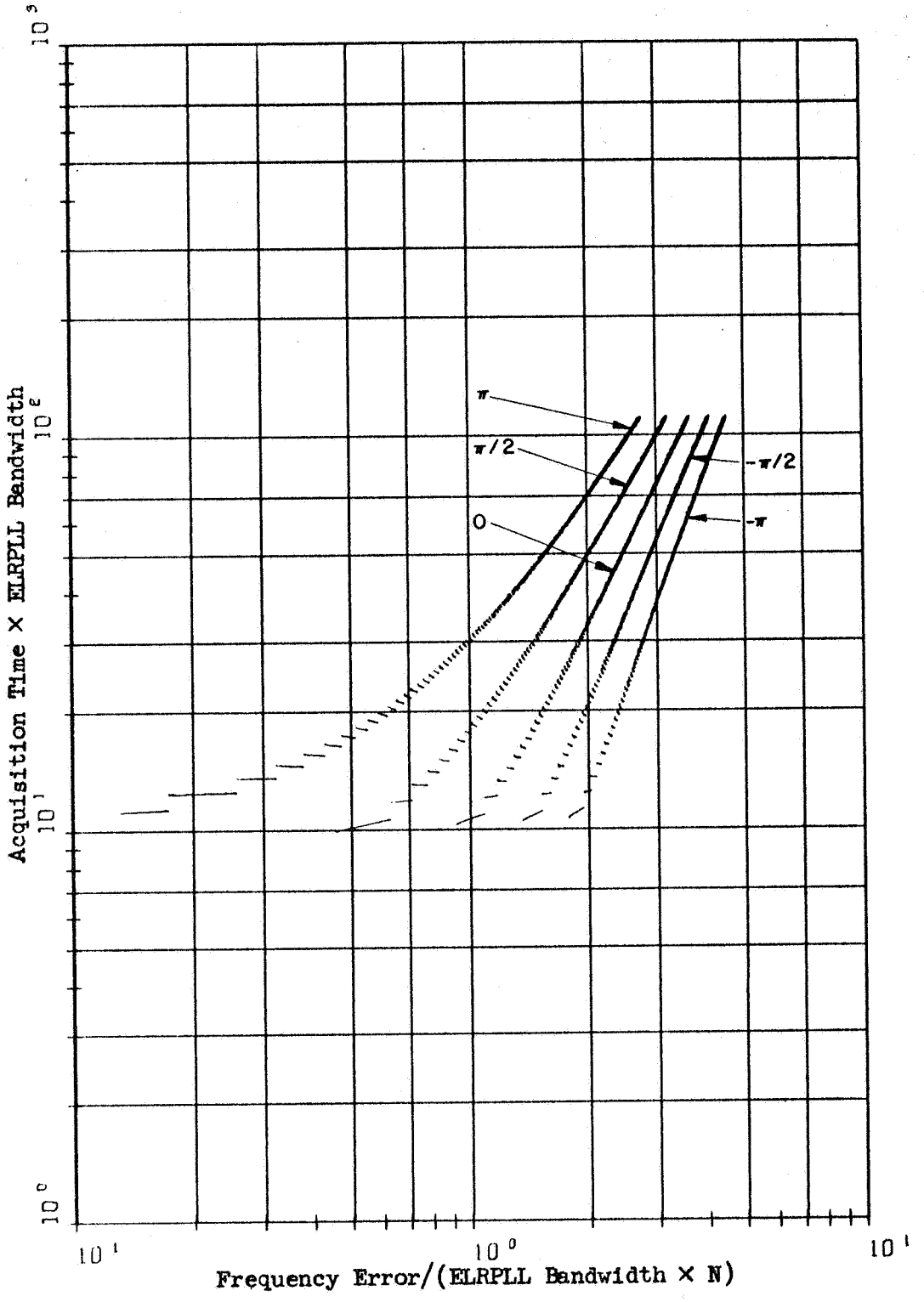

Figure 3.6. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to 1.4

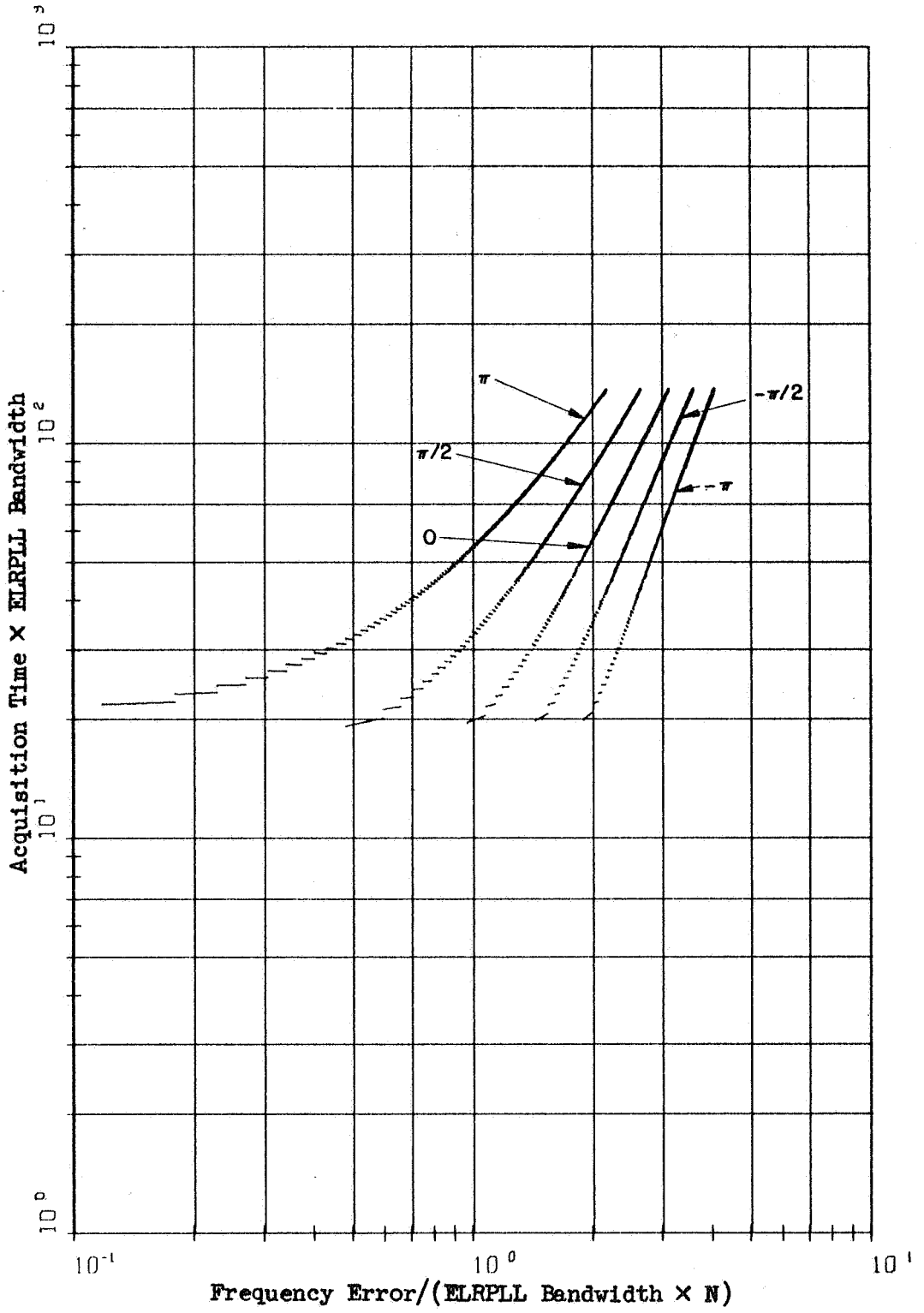

Figure 3.7. ELRPLL Acquisition Time versus the Initial Frequency Error and Phase Error for a Damping Ratio Equal to 2

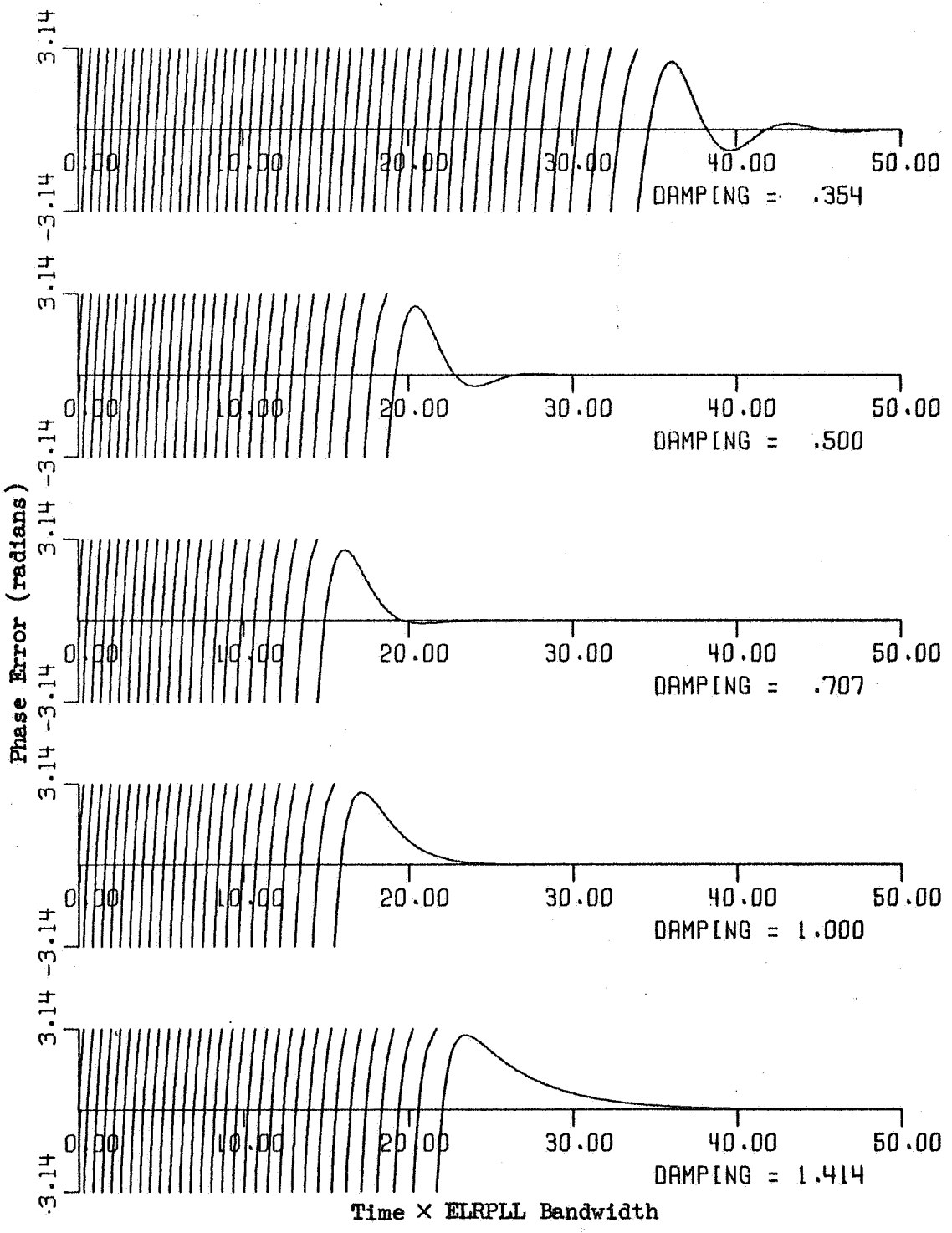

Figure 3.8. High S/N ELRPLL Transient Phase Error for Zero Initial Phase Error and Frequency Error = 2 for Several Damping Ratios

point. The slope at successive peaks of the phase error is a monotonically decreasing function of time. This condition is necessary to guarantee acquisition.

3.6. ELRPLL Acquisition Time

Figure 3.8 shows that the acquisition time of the ELRPLL has a minimum for $\xi = .707$. An analysis of Viterbi's [31] expression for the acquisition time of a PLL with sinusoidal phase detector characteristic reveals that its acquisition time also exhibits a minimum for $\xi = 1/\sqrt{2}$.

His expression after changing notation is

$$T_s' \simeq 4\pi^2 T_1 B_L [\Delta f'(0)]^2/K \tag{3.35}$$

which is assymptotically accurate for large $\Delta f'(0)$. Using equations (2.16) and (3.6) in (3.35), (3.36) is obtained.

$$T_s' \simeq \pi^2(1 + 4\xi^2)^3 [\Delta f'(0)]^2/32\xi^4 \tag{3.36}$$

Differentiating T_s' with respect to ξ, setting the result to zero and solving for ξ, the minimum $T_s'[\Delta f'(0)]$ is found to occur at $\xi = 1/\sqrt{2}$.

Figure 3.9 is a plot of $T_a'[\Delta f'(0)]$ for $\Phi_e(0) = 0$ and several values of ξ for the ELRPLL. It is apparent from the slope of the plots that T_a' has a quadratic dependence on $|\Delta f'(0)|$ and that T_a' also has a minimum at $\xi = .707$ for any T_a' such that $10 < T_a' < 1000$. From these observations and intuitive reasoning it is hypothesized that

$$T_a' = K_1 T_s'/N^2 \tag{3.37}$$

or that

$$T_a' \simeq K_1 \pi^2(1 + 4\xi^2)^3 [\Delta f'(0)]^2/32\xi^4 N^2 \tag{3.38}$$

for $|\Delta f'|/N > 1$. This hypothesis is tested by determining K_1 for one

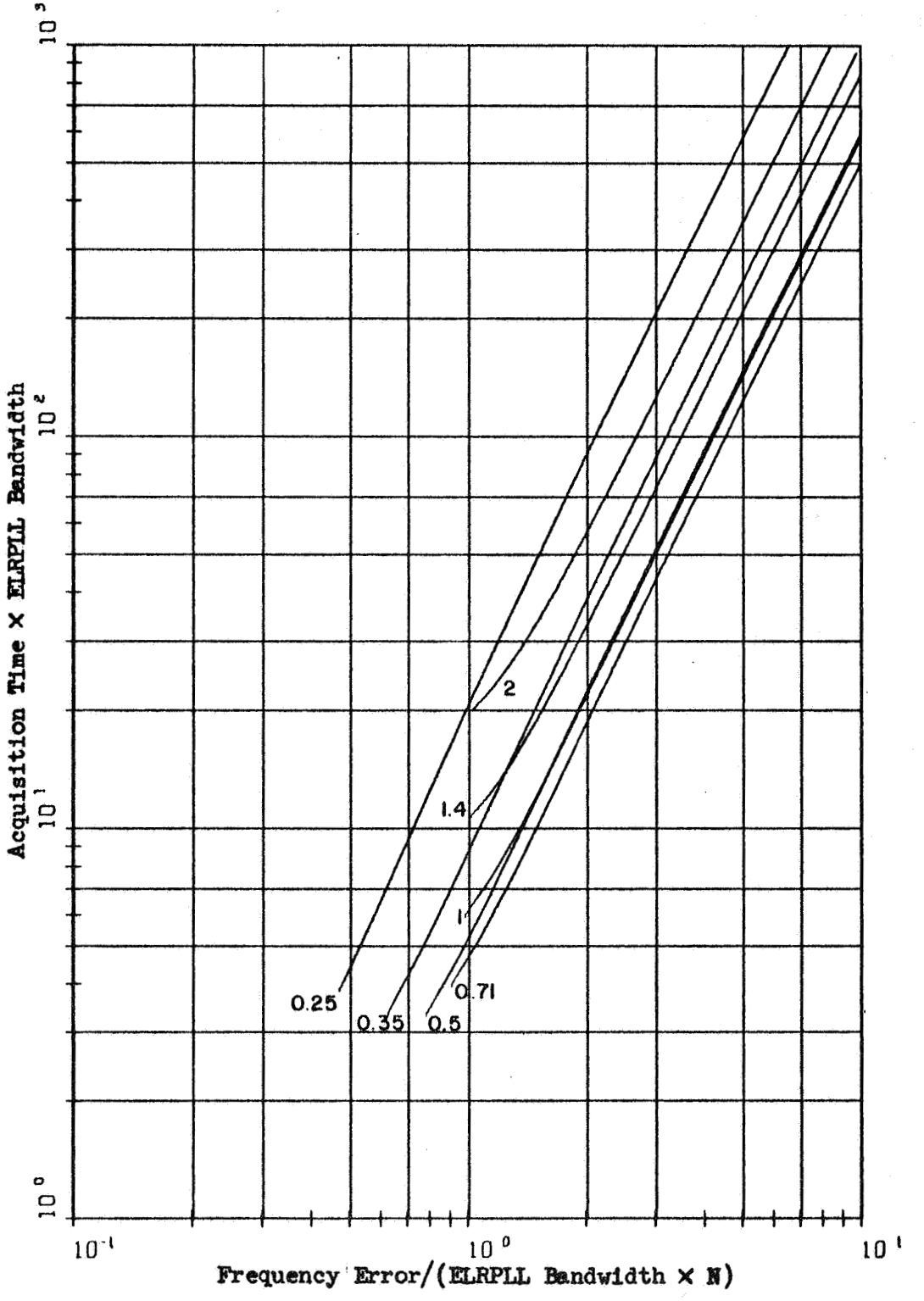

Figure 3.9 ELRPLL Acquisition Time versus the Initial Frequency Error and Damping Ratio for an Initial Phase Error = 0

value of ξ from Figure 3.9 and then comparing (3.38) with Figure 3.9 for several values of ξ. T_a' for $\xi = 1$, $N = 1$, and $|\Delta f'|/N = 2$ is 23. Therefore

$$K_1 = 23 \cdot 32 \xi^4 N^2/\pi^2(1 + 4\xi^2)^3 \Delta f'^2 \doteq .149 \qquad (3.39)$$

Table 3.1 compares (3.38) and Figure 3.9 using $K_1 = .149$ for $N = 1$ and $\Delta f' = 2$.

Table 3.1

Verification of Acquisition Time Model Hypothesis

ξ	T_a'	Figure 3.9	Equation (3.38)
.35		39	39.8
.5		23	23.6
.707		19	19.9
1.0		23	23
1.44		34	33.5

Note that the comparison in Table 3.1 is very favorable. Hence it is concluded that (3.38) for $K_1 = .149$ is a good model for the ELRPLL high S/N acquisition time when $|\Delta f'|/N > 2$.

IV. ELRPLL SYSTEM SIGNAL GENERATOR AND CHANNEL

This chapter along with Appendix B describes the experimental ELRPLL system built for and used in this study. The block diagram of the system is presented and the system is discussed. The circuits and other technical considerations including system accuracy are discussed in Appendix B.

A description of the transmitter or signal generator and the channel is also included. The circuit diagrams and technical considerations of this test fixture including system accuracy are in Appendix C.

4.1. Experimental ELRPLL System

The novel feature of the ELRPLL is the phase detector. Section 1.2.3 describes several ways of implementing this phase detector. An attempt was made to use the Geda analog computer to simulate the ELRPLL. However this did not work properly. Therefore it was decided to build an ELRPLL in the laboratory. Figure 4.1 is a block diagram of the experimental ELRPLL system showing the way in which the phase detector is implemented. The linear modulo $2N\pi$ characteristic is synthesized in three steps. One part of the system determines the modulo $\pi/2$ phase error, a second part adds the quadrant information, and the third part determines the modulo N number of 2π radian cycle slips.

The system input is J2 and the normal output as a FM demodulator is J18. A pair of reference square waves in phase quadrature are generated from the multivibrator VCO by a pair of flip-flops triggered by

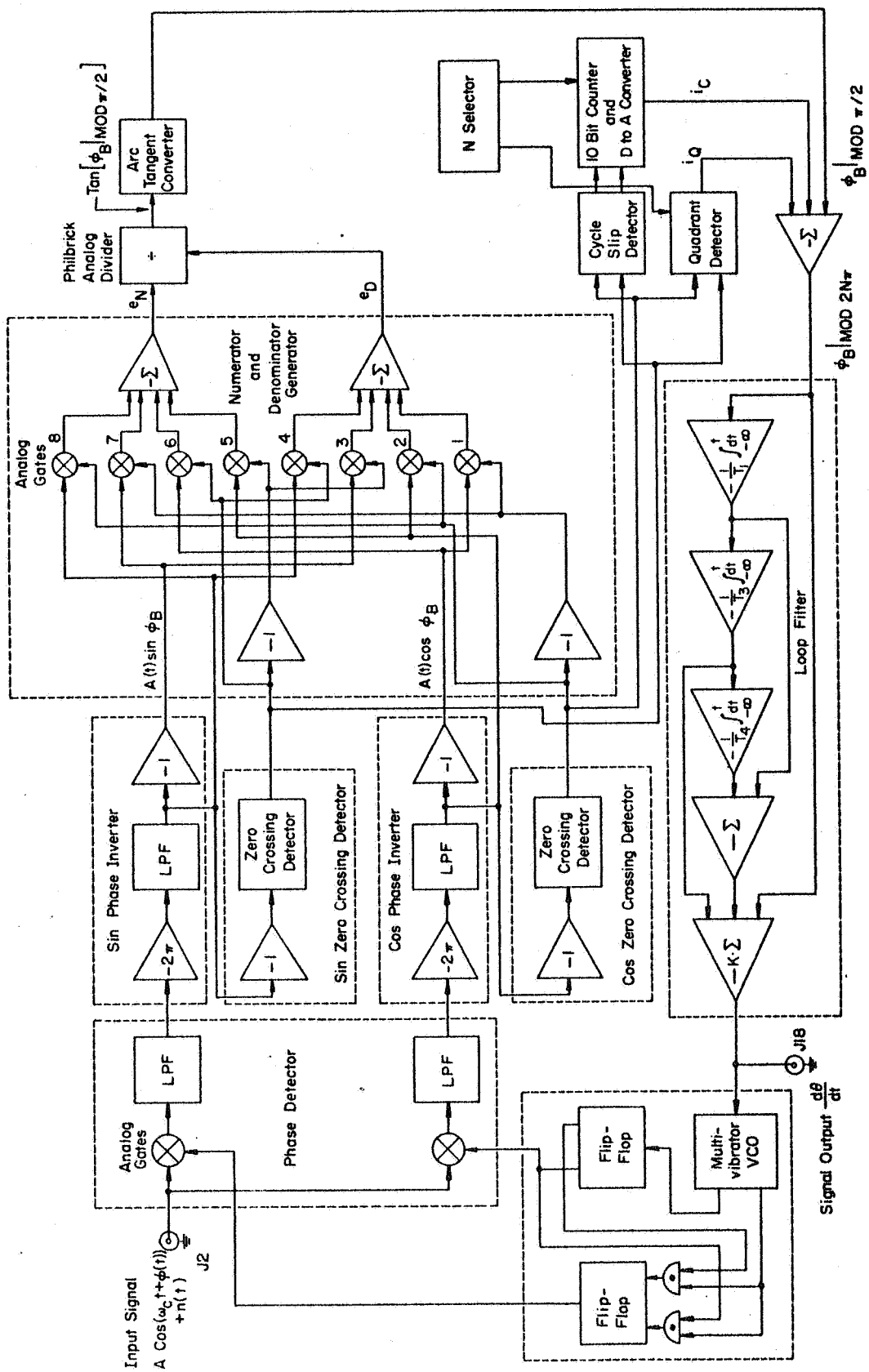

FIGURE 4.1 DETAILED ELRPLL BLOCK DIAGRAM.

the VCO output transitions. One of the flip-flops functions as a frequency divide by 2 circuit and is used as a control for the other. The control is such that the left flip-flop output always leads that of the right by 1/4 of a period.

The phase detector consists of 2 analog gates and LPFs. The gates are open when the reference is positive and are closed otherwise. The LPFs are designed for a cutoff frequency of $f_c/10 \simeq 10KHz.$ so as to provide adequate rejection of the carrier and all higher frequency cross products. Let the input signal be

$$r(t) = A\ \mathrm{Cos}[\omega_c t + \phi(t)] + n(t), \tag{4.1}$$

where $\dot{\phi}(t)$ is the modulation waveform and $n(t)$ is the channel noise. Let the VCO references have frequency, $\omega_v + \dot{\theta}(t)$, where $\dot{\theta}(t)$ is the VCO input waveform. Then the output of the upper LPF is

$$e_s = -\frac{A(t)}{2\pi}\ \mathrm{Sin}[(\omega_c - \omega_v)t + \phi(t) - \theta(t) + \psi(t)] \tag{4.2}$$

and the output of the lower LPF is

$$e_c = -\frac{A(t)}{2\pi}\ \mathrm{Cos}[(\omega_c - \omega_v)t + \phi(t) - \theta(t) + \psi(t)], \tag{4.3}$$

where

$$A(t) = [(A + n_1(t))^2 + n_2^{\,2}(t)]^{.5} \tag{4.4}$$

and

$$\psi(t) = \mathrm{Tan}^{-1}\{n_2(t)/[A + n_1(t)]\}. \tag{4.5}$$

$n_1(t)$ and $n_2(t)$ are obtained by splitting $n(t)$ into two components that are in phase and out of phase with the modulated signal, $A\ \mathrm{Cos}[\omega_c t + \phi(t)]$.

The Sin and Cos Phase Inverters provide isolation of the analog gates from the Numerator and Denominator Generator (NDG) as well as

further filtering of the phase detector outputs. They also produce a phase inversion that is needed by the Sin and Cos Zero Crossing Detectors. These Zero Crossing Detectors generate binary signals that depend only on the sign of their inputs.

The output of the Inverters and Zero Crossing Detectors are used by the NDG. The NDG is an analog multiplexor. Each of the eight analog gates is open when the appropriate binary signal from one of the Zero Crossing Detectors or from one of the sign changers within the NDG is positive. The numerator output is

$$e_N = A[\mathrm{Sin}\phi_B \ \mathrm{SGN}(\mathrm{Cos}\phi_B) - \mathrm{Cos}\phi_B \ \mathrm{SGN}(\mathrm{Sin}\phi_B)] \ , \tag{4.6}$$

and the denominator output is

$$e_D = -A[\mathrm{Sin}\phi_B \ \mathrm{SGN}(\mathrm{Sin}\phi_B) + \mathrm{Cos}\phi_B \ \mathrm{SGN}(\mathrm{Cos}\phi_B)] \ , \tag{4.7}$$

or more simply

$$e_D = -A[|\mathrm{Sin}\phi_B| + |\mathrm{Cos}\phi_e|]. \tag{4.8}$$

These two outputs are designed so that

$$-\frac{e_N}{e_D} = \mathrm{Tan}[(\phi_B + \pi/4)_{\mathrm{Mod}\ \pi/2} - \pi/4]. \tag{4.9}$$

The Philbrick Analog Divider performs this operation. The Arc Tangent Converter output is $[\phi_B + \pi/4]_{\mathrm{Mod}\ \pi/2} - \pi/4$.

There are several reasons why it was decided to calculate the modulo $\pi/2$ phase error. The method is not sensitive to the value of A and it permits the studying of the case for N = .25 and .5.

Since the denominator input to the divider is always less than zero except for very short times when both inputs go to zero, in theory the divider output never saturates. In practice it seldom saturates.

The Zero Crossing Detector outputs are also used by the Quadrant Detector. This device generates a signal proportional to the quadrant of the modulo 2π phase. This signal is

$$i_Q = [\phi_B + \pi]_{\text{Mod } 2\pi} - [\phi_B + \pi/4]_{\text{Mod } \pi/2} - 3\pi/4. \qquad (4.10)$$

The Cycle Slip Detector detects each time $\phi_e|_{\text{Mod } 2\pi} = 2\pi$ and generates an "add" or "subtract" pulse. If $\dot{\phi}_e > 0$, an add pulse is generated and a subtract pulse if $\dot{\phi}_e < 0$. The case of $\dot{\phi}_e = 0$ is irrelevant since $\phi_B|_{\text{Mod } 2\pi}$ cannot pass 2π for $\dot{\phi}_e = 0$. These pulses are counted and the instantaneous modulo N count of the number of positive minus negative pulses is stored by the 10 Bit Counter. However the number of bits used can be varied and hence N can be changed in steps of 2 to 1 ratio from .25 up to 1024. The D to A converter in the counter generates a current related to the instantaneous count. If the count in the counter is N_1

$$i_c = [N_1 - N/2 + .5]_{\text{Mod } N} + N/2. \qquad (4.11)$$

The output signal is translated by $N/2 + .5$ so that the output is symmetric about the origin. This generates a symmetric phase detector characteristic with a range of $N\pi$ radians in both the positive and negative directions.

The three components of the phase error modulo $2N\pi$ are summed in the lower right hand corner block. The output of this summer drives the loop filter. The loop filter consists of five operational amplifiers; three of which are connected as integrators and the remaining two as summers. The time constants of the three integrators are T_1, T_3 and T_4. The time constant and initial condition of each integrator can be set independently of the others. By setting T_1 through T_4 to ∞ the system is a first order

loop. If T_1 is then made finite the system is a second order loop with ideal integrator. Then if T_3 is made finite the system is a third order loop, and finally if T_4 is made finite the system is a 4th order loop. The loop gain can be changed by varying K. The transfer function of the loop filter is

$$F(s) = K\left\{1 + \frac{1}{T_4 s}\left[1 + \frac{1}{T_3 s}\left(1 + \frac{1}{T_1 s}\right)\right]\right\} . \qquad (4.12)$$

The loop filter output, $\dot{\theta}(t)$, is an estimate of the modulation waveform and is available at J18 as a loop output signal. It also determines the VCO frequency. With this system first and second order ELRPLL with bandwidths from 1 Hz. to 1000 Hz. can be simulated. For second order loops a wide range of damping ratios can be accommodated. The third and fourth order loops are not considered in this study, but they can be simulated by the system.

4.2. Experimental Signal Generator and Channel

This section describes the block diagram of the Signal Generator and Channel. The details of this system are contained in Appendix C.

The experiments planned for the ELRPLL require the use of an accurate stable signal generator with calibrated FM and additive, band-limited, white, gaussian channel noise. Since there was no readily available device meeting the requirements, the system shown in Figure 4.2 was built in the laboratory.

The VCO frequency is controlled by the sum of the modulation attenuator and carrier frequency set outputs. The output level of the VCO is set by an attenuator and added to the attenuated input noise. The spectrum of this gaussian noise is essentially flat up to 200 KHz. The combined signal is passed through a band pass filter with a center

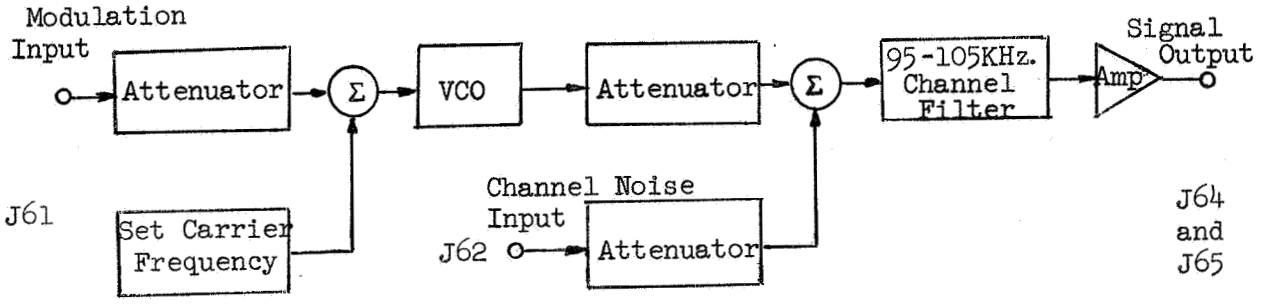

Figure 4.2. Signal Generator and Channel.

frequency of 100 KHz. and a 3 db bandwidth of 10 KHz. This filter has a 7 pole butterworth response. Its purpose is to simulate the band pass of the receiver that normally preceeds a PLL. The output amplifier increases the signal plus noise level so that its maximum amplitude is 3 V RMS.

The S/N level at the output can be varied over a -60 to 60 db range, and the frequency over a range of 95 to 105 KHz.

V. EXPERIMENTAL ACQUISITION TIME

This chapter describes the acquisition time experiment for the ELRPLL and presents the experimental results. An approximate acquisition time model is presented and discussed.

One of the most important parameters of any PLL system is its acquisition time. Often the carrier frequency of a received signal is unknown because of doppler shift. If the S/N level in a band sufficiently large to include the unknown frequency carrier, is much less than 0 db it can be very difficult to locate the carrier and determine its frequency.

One of the uses of a PLL is to determine the frequency of such a signal. However, it is often necessary that this acquisition take place as quickly as possible. Viterbi [31] has shown that when the S/N is large the acquisition time of a PLL is proportional to the square of the frequency error. In Chapter III it is also found to be true for the ELRPLL. A search of the literature revealed no theoretical or experimental model for the low S/N second order PLL acquisition time. Uhran [27] gives some experimental data for the first order PLL. Therefore a great amount of time was spent in determining an acquisition time model. This model includes the effect of loop bandwidth, damping ratio and N, VCO frequency error, S/N level and carrier frequency.

Section 5.1 describes the experiment. Section 5.2 presents the experimental data and Section 5.3 presents and discusses a regression

analysis model obtained for the ELRPLL.

5.1. Acquisition Time Experiment

Acquisition time is defined rather loosely in the literature as the length of time needed for a PLL to acquire synchronization. In this study a measurable criteria is defined by (2.9), (2.10), and (2.11). The first equation limits the maximum frequency error to $B_L/2$ for acquisition to be completed. The second requires that the initial and final frequency errors need to be of opposite sign and the last requires that the phase error be less than one twentieth of the phase error range.

Figure 5.1 is a block diagram of the Acquisition Time Experimental Set Up. The block diagram of the ELRPLL and Loop Control System is Figure 5.2. The control system consists of six level detectors, coincidence logic and a control system. The level detectors are connected to various points in the ELRPLL system. One is connected to J28 and is used to test when the phase error passes through zero. When this occurs the coincidence logic generates a start output and closes the loop filter relays RL_1 through RL_4 and opens the initial condition applying relays RL_5 through RL_7. This determines the initial phase and frequency errors. The start output also starts the counter timer. Two more level detectors are used to determine when (2.9) through (2.11) are satisfied. When this occurs the coincidence logic generates a stop pulse to stop the timer and open RL_1 through RL_4. This puts a "hold" on the integrators in the loop filter. The coincidence logic, when in the automatic mode, automatically resets the control system after one second and repeats the above

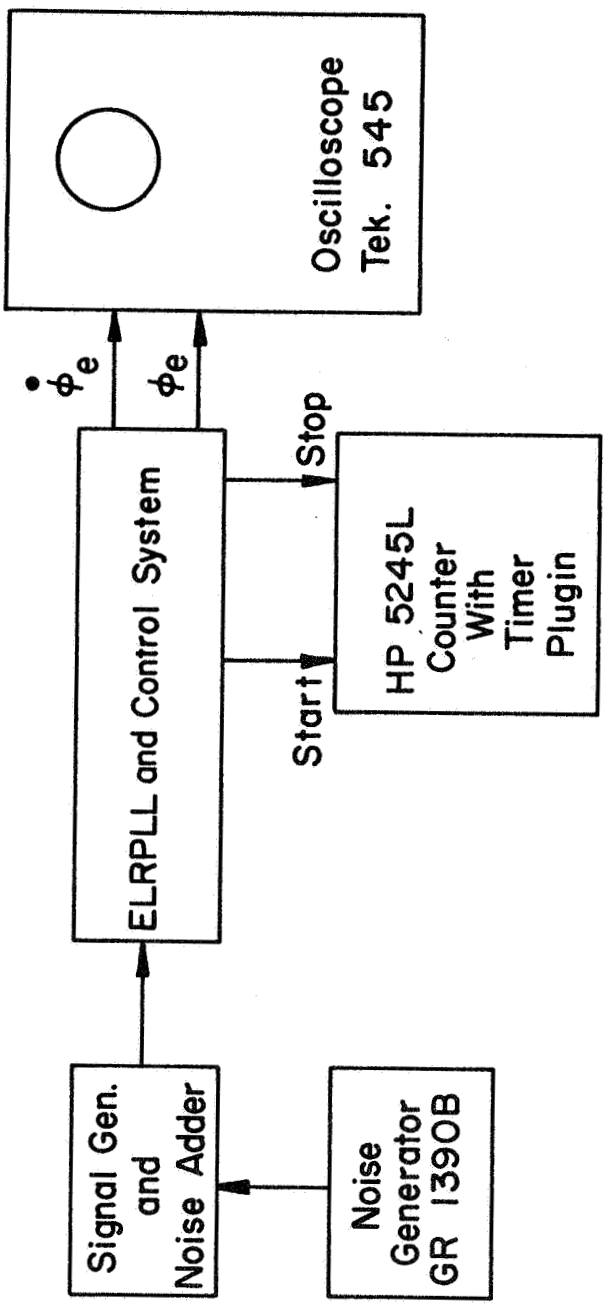

FIGURE 5.1. ACQUISITION TIME EXPERIMENTIAL SET UP.

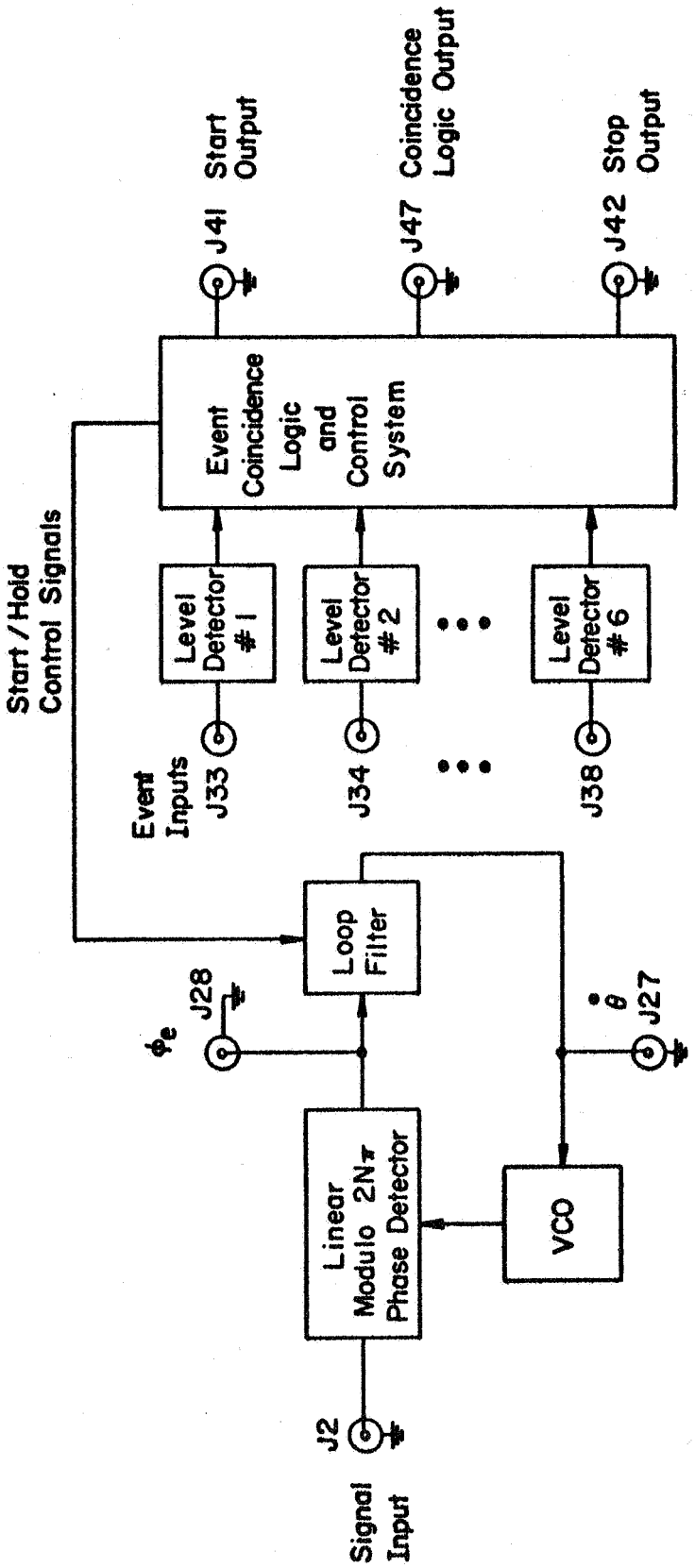

FIGURE 5.2. ELRPLL AND LOOP CONTROL SYSTEM.

process. This facilitates the taking of data. If noise is included in the ELRPLL input it is necessary to take several samples at each parameter point in order to determine the statistics of the acquisition time. Further information concerning the operation and description of this control system is contained in Appendix D.

Using this system, statistical acquisition time data is obtained for several ELRPLL and signal parameter values. The parameters that are varied are the ELRPLL damping ratio, the phase error range constant N, the S/N level, the initial frequency error and the carrier frequency.

5.2. Acquisition Time Data

This section presents the normalized acquisition time data. This data is plotted as a function of N/S level on log/log plots. Each graph has a legend giving the values of ξ, B_L, $\Delta f'$, and N. There are separate graphs for different values of carrier frequency. The carrier frequency is normalized with respect to the IF center frequency and bandwidth.

$$f_c' = \frac{f_c - f_0}{B_{IF}} \quad . \tag{5.1}$$

The low S/N acquisition time data is normalized with respect to the high S/N acquisition time data to facilitate a comparison of the data for different parameter values. The S/N level is normalized with respect to the ELRPLL bandwidth B_L.

Since there is a large number of data sets for the cases of $f_c' = 0$ and .1, two graphs each are used to present this data.

Figures 5.3 through 5.9 are the graphs of the normalized acquisition time versus the N/S levels. For most cases the acquisition increases with decreasing S/N level. The few exceptions are for certain cases when

CURVE	DAMPING	BANDWIDTH	DF	N
⏲	.5	60	16.67	1
Δ	.5	75	1.33	1
+	1.0	75	-2.67	1
X	1.0	75	-1.33	1
◇	1.0	75	1.33	1
✦	1.0	75	2.67	1
⧖	1.0	75	13.33	1
Z	2.0	75	1.33	1
Y	2.0	127	7.84	1
⌑	.5	60	16.67	2
✳	1.0	75	1.33	2
⧖	1.0	75	13.33	2
I	2.0	75	1.33	2
⧓	2.0	127	7.84	2

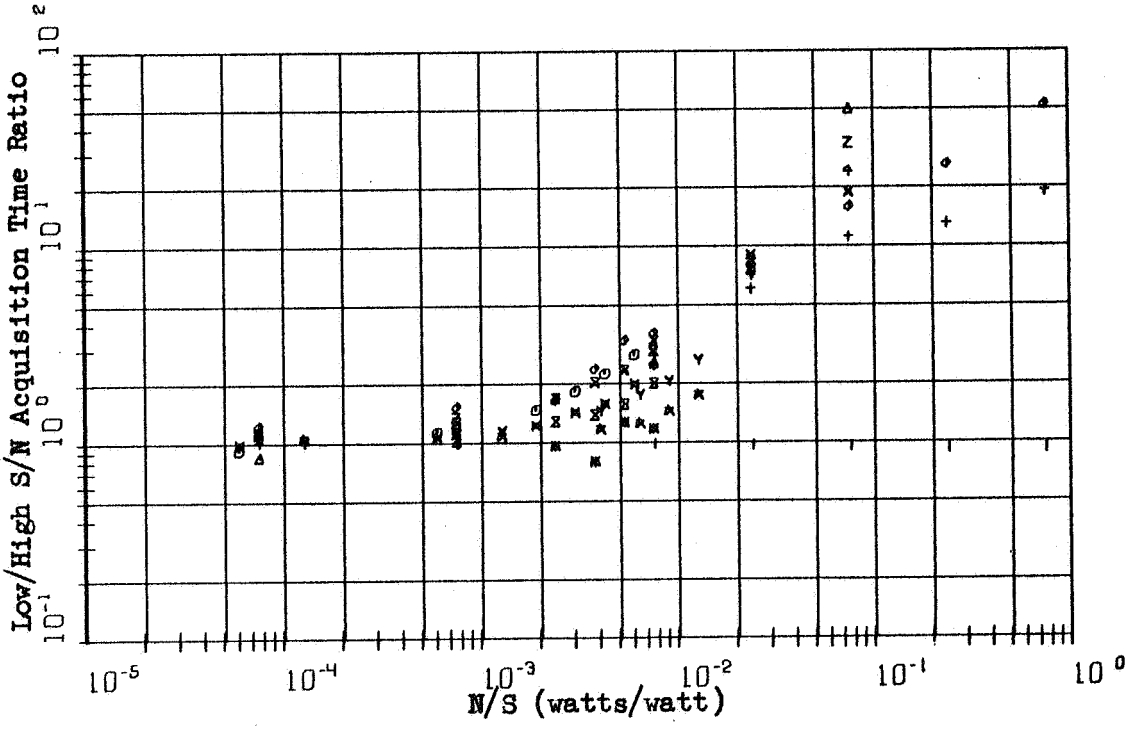

Figure 5.3. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of 0 Hz. Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	DF	N
○	.5	60	16.67	4
△	1.0	75	13.33	4
+	2.0	127	7.84	4
X	.5	60	16.66	8
◇	1.0	75	13.34	8
✦	2.0	127	7.84	8
X	.5	60	16.67	16
Z	1.0	75	13.33	16
Y	.5	60	16.67	32

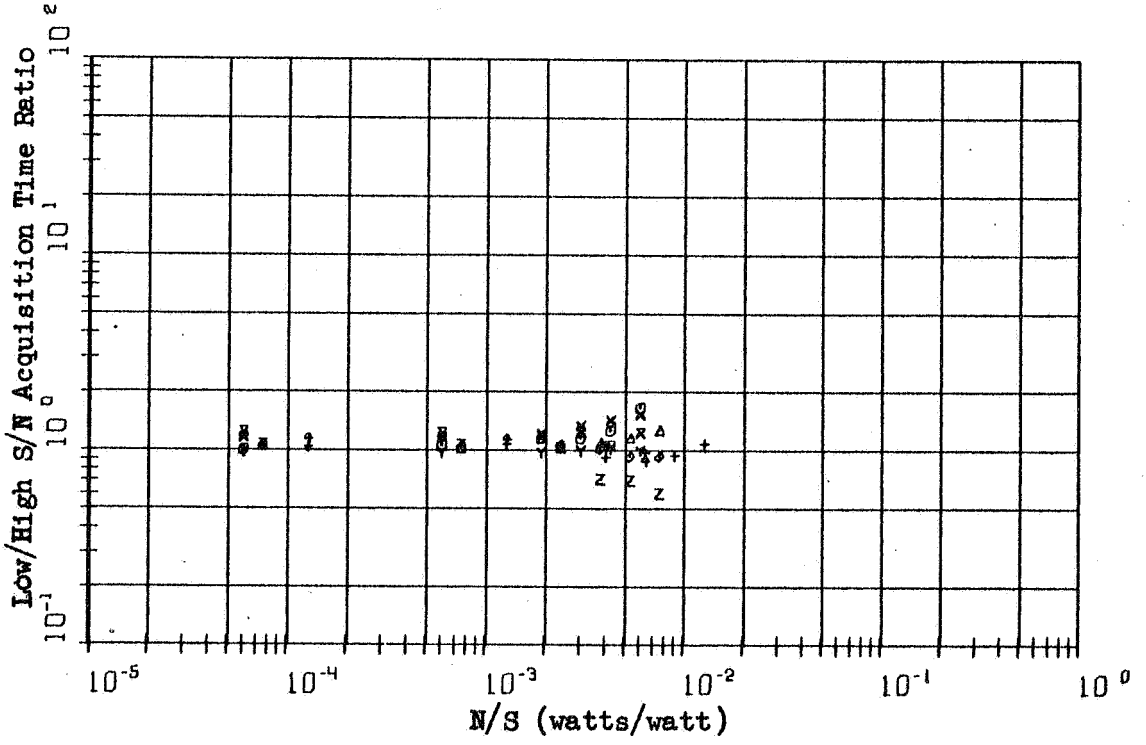

Figure 5.4. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of 0 Hz. Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	DF	N
⊙	.5	60	-16.67	1
△	1.0	75	-13.33	1
+	1.0	75	-1.33	1
×	1.0	75	1.33	1
◇	1.0	75	2.67	1
✦	1.0	75	13.33	1
⊠	2.0	127	-7.84	1
Z	.5	60	-16.67	2
Y	1.0	75	-13.33	2
⌑	1.0	75	-1.33	2
✳	1.0	75	1.33	2
⧖	1.0	75	13.33	2
I	1.0	75	13.33	2

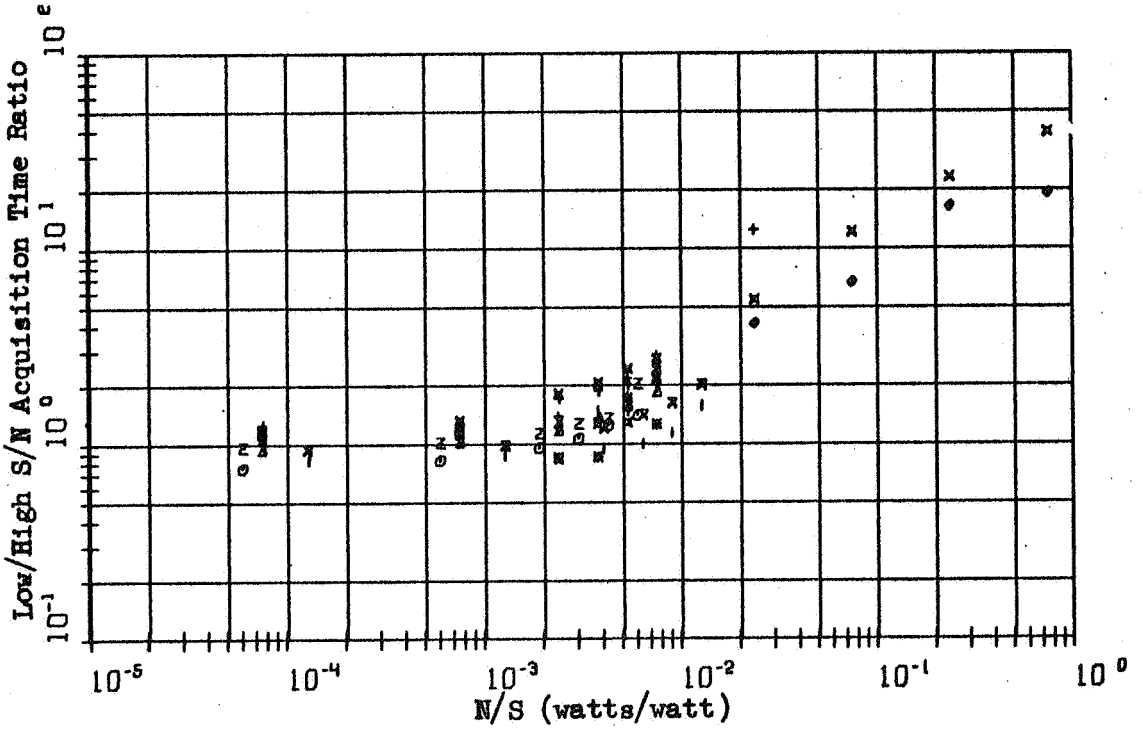

Figure 5.5. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of .1 Hz, Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	DF	N
⊙	.5	60	-16.67	4
△	1.0	75	-13.33	4
+	1.0	75	13.33	4
X	2.0	127	-7.84	4
◇	.5	60	-16.66	8
✦	1.0	75	-13.34	8
X	1.0	75	13.34	8
Z	2.0	127	-7.84	8
Y	.5	60	-16.67	16
⌘	1.0	75	-13.33	16
✱	1.0	75	13.33	16
⧖	.5	60	-16.67	32

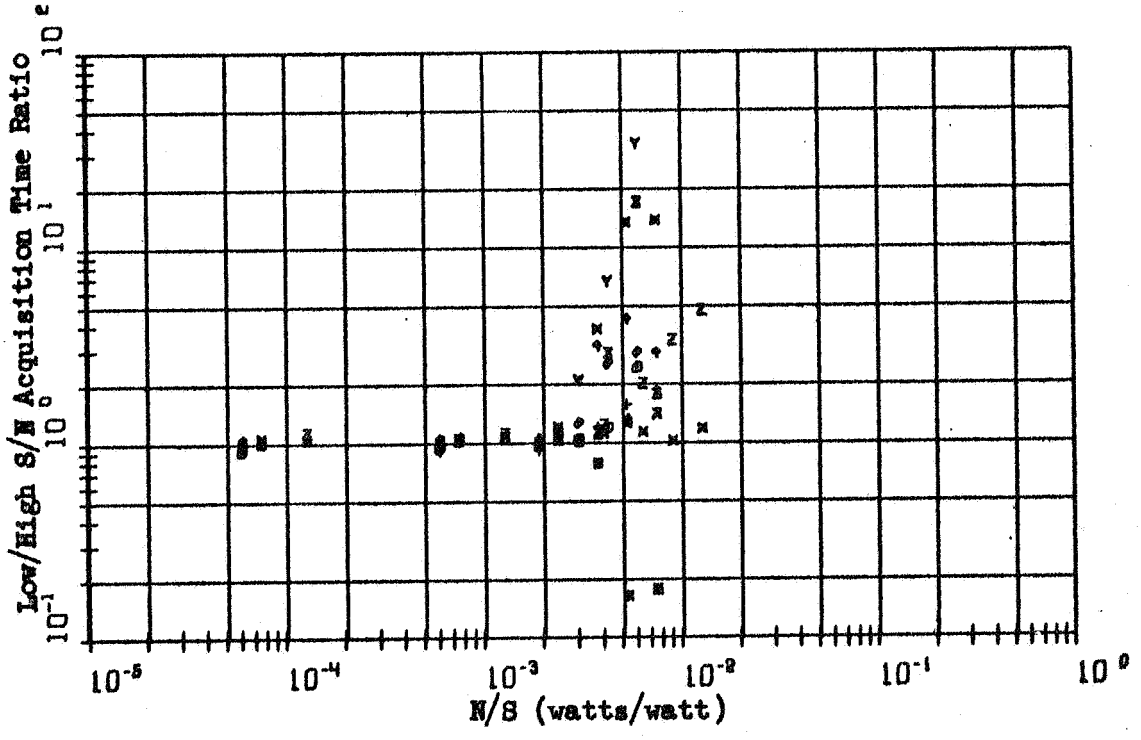

Figure 5.6. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of .1 Hz. Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	DF	N
⊙	.5	60	-83.32	4
△	1.0	75	-66.68	4
+	2.0	127	-39.22	4
×	.5	60	-83.36	8
◇	1.0	75	-66.66	8
⊕	2.0	127	-39.22	8
X	.5	60	-83.33	16
Z	1.0	75	-66.67	16
Y	2.0	127	-39.22	16
⊠	.5	60	-83.33	32
✳	1.0	75	-66.66	32
⧖	2.0	127	-39.20	32
I	.5	60	-83.33	64
⋈	1.0	75	-66.69	64
—	2.0	127	-39.21	64
I	.5	60	-83.33	128

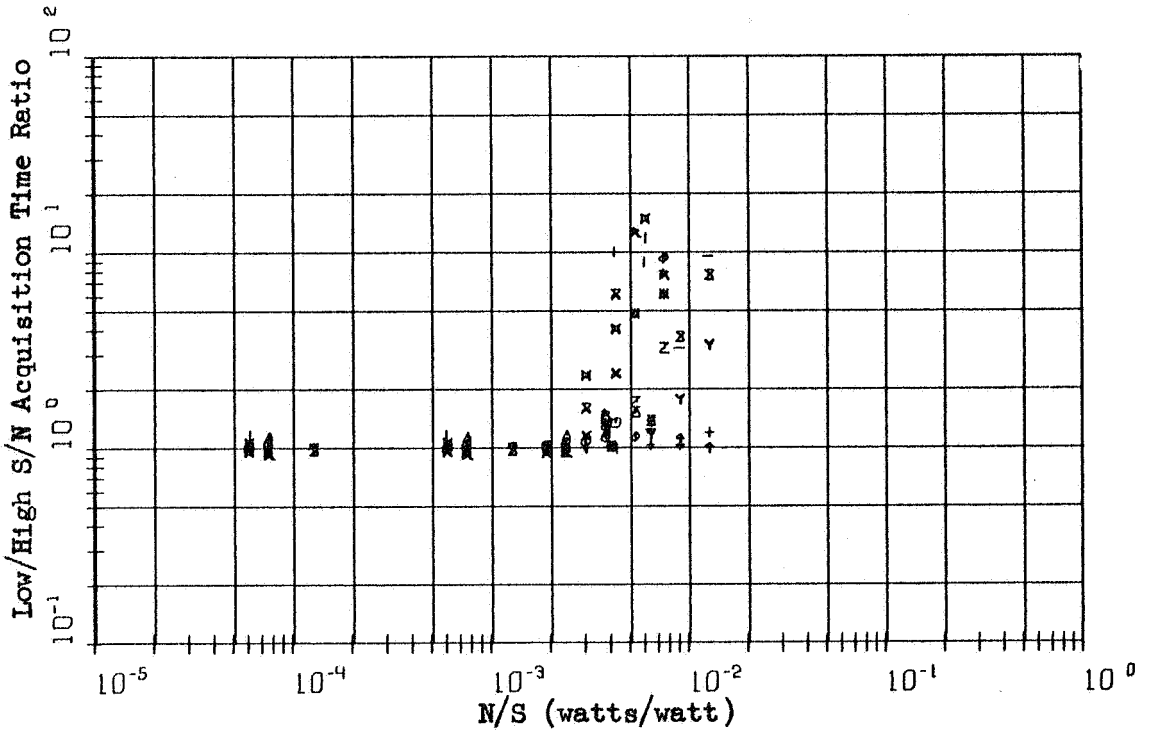

Figure 5.7. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of .25 Hz. Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	OF	N
⊙	1.0	75	-13.33	1
△	1.0	75	-2.67	1
+	1.0	75	-1.33	1
×	1.0	75	1.33	1
◇	1.0	75	2.67	1
✦	1.0	75	13.33	1
X	1.0	75	-13.33	2
Z	1.0	75	-1.33	2
Y	1.0	75	1.33	2
⌘	1.0	75	13.33	2
✳	1.0	75	-13.33	4
⧖	1.0	75	13.33	4
I	1.0	75	-13.34	8
⋔	1.0	75	13.34	8
–	1.0	75	-13.33	16
I	1.0	75	13.33	16

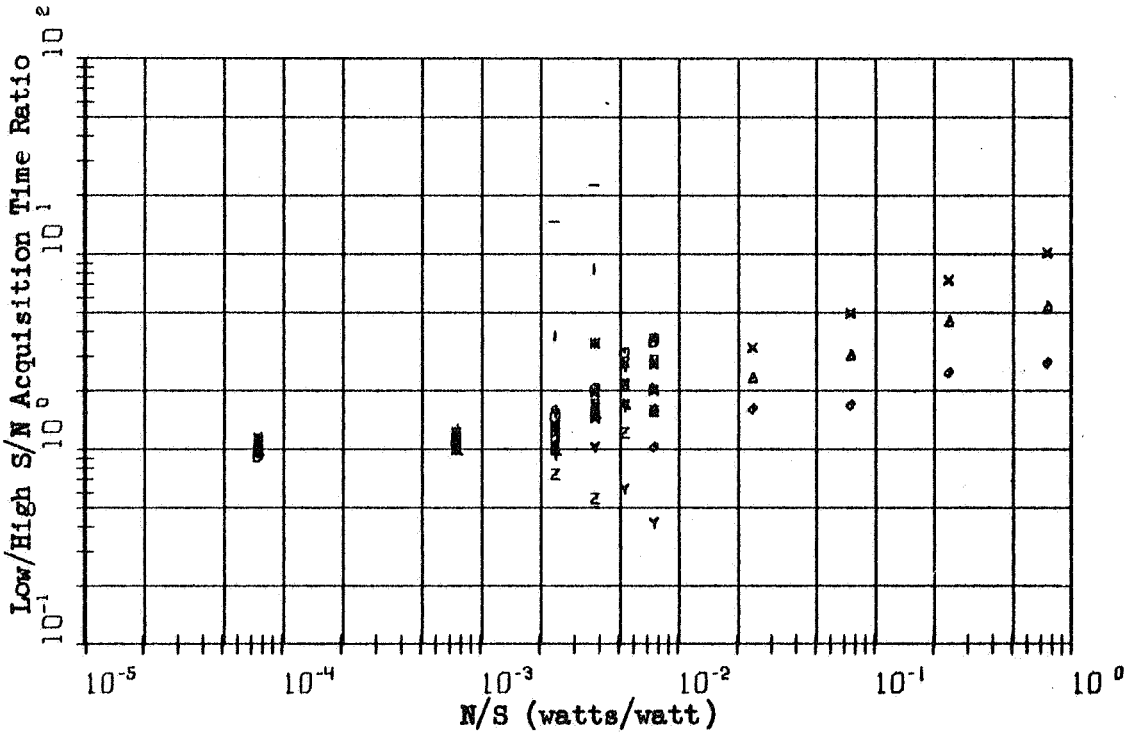

Figure 5.8. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of .3 Hz. Carrier Frequency Offset

CURVE	DAMPING	BANDWIDTH	DF	N
⊙	.5	60	-16.67	1
△	1.0	75	-13.33	1
+	2.0	127	-7.84	1
×	.5	60	-16.67	2
◇	1.0	75	-13.33	2
✦	2.0	127	-7.84	2
⊠	.5	60	-16.67	4
Z	1.0	75	-13.33	4
Y	2.0	127	-7.84	4
⊡	.5	60	-16.66	8
✳	1.0	75	-13.34	8
⧖	2.0	127	-7.84	8
I	.5	60	-16.67	16
⊛	1.0	75	-13.33	16
—	.5	60	-16.67	32

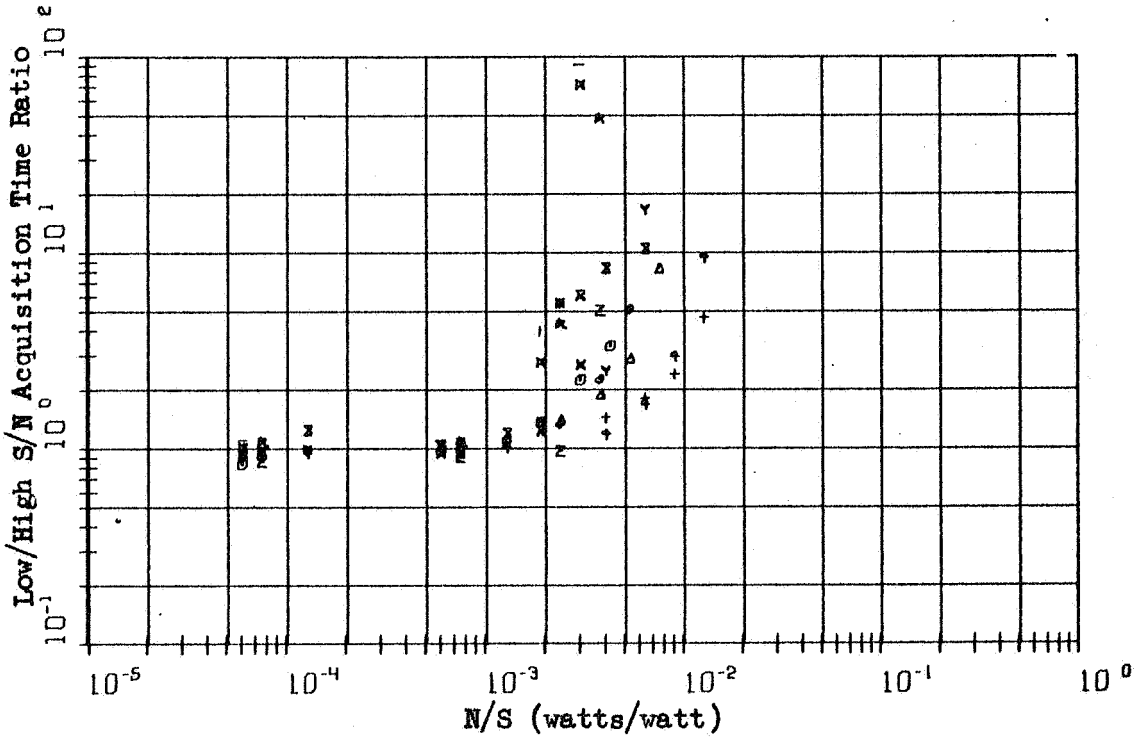

Figure 5.9. Second Order ELRPLL Acquisition Time versus S/N in ELRPLL Bandwidth for the Case of .5 Hz. Carrier Frequency Offset

$$f_0 \leq f_c < f_v \tag{5.2}$$

or

$$f_0 \geq f_c > f_v. \tag{5.3}$$

For either case the majority of the noise generated cycle slips are in the opposite direction as those due to frequency error. It is proposed that this condition tends to decrease the acquisition time but the mechanism is not well understood.

The slope of T_a with respect to N/S is strongly dependent on f_c and N. For large N and f_c this slope is greatest and for small N and large f_c the rate is small. For small f_c the slope is a decreasing function of N.

5.3. Acquisition Time Model

This section introduces a mathematical curve fitting procedure called regression analysis, and presents a mathematical model that predicts the average acquisition time as a function of several ELRPLL system and signal parameter values.

Regression analysis [8] is a technique whereby a mathematical model for predicting an event can be determined from experimental measurements of that event. The user must supply a model with undetermined coefficients. These are optimized by the regression so that the model fits the data with a minimum square error goodness of fit.

Ideally, one needs to know the nature of the model. When this is not known, intuition based on examination of the data must be employed to determine an initial model. After trying to optimize this model, one can analyze the residuals or differences between the data and the

prediction to obtain ideas for improving the nature of the model. This process is repeated until the desired degree of accuracy is attained.

A disadvantage of regression analysis is that the models obtained are usually very complex because their true nature is unknown and must often be guessed. Therefore a digital computer is often necessary to interpret the model.

An advantage of regression analysis is that it simplifies interpolation between the original data points. This is very difficult to do without a model when the data is stocastic, or if a multidimensional, or multiple order interpolation is desired. However the regression model is not useful for extrapolation beyond the data.

To be more precise let there be L data samples. Let X_i be a 6 element column vector where its elements are the values of six parameters of the ELRPLL and the signal for the ith sample. Let $\hat{T}_a(X_i, B)$ be the model for the predicted acquisition time where B is a K component vector of parameters to be optimized. The criteria of optimality is the minimization of

$$\epsilon = \sum_{i=1}^{L} \left[T_{ai} - T_a\left(X_i, B\right) \right]^2 w_i, \tag{5.4}$$

where w_i is the weighting associated with the ith data sample, T_{ai}. Throughout this study the weighting used is the inverse of the variance of the data sample. For this reason 10 data samples are taken at each point in the parameter space. These are averaged to determine T_{ai}. The variances of the sample means are also calculated. These are used to determine the weights. The variable R^2 is a commonly used goodness of fit criteria. It is given by

$$R^2 = 1 - \epsilon \Big/ \sum_{i=1}^{L} \left(T_{ai} - \bar{T}_a \right)^2, \tag{5.5}$$

where

$$\bar{T}_a = \frac{1}{L} \sum_{i=1}^{L} T_{ai} w_i \ . \tag{5.6}$$

A perfect fit yields an $R^2 = 1$. $\hat{T}_a(X_i, B) = \bar{T}_a$ yields $R^2 = 0$. R^2 is analogous to the square of the commonly used correlation coefficient ρ.

A non-linear regression analysis computer program called NONLIN and a linear regression analysis program called WRAP obtained from the Purdue University Statistics Department are used to select B such that (5.4) is minimized. WRAP is used to analyze the high S/N subset of the data for several models. It is found that a modification of Viterbi's [31] result for lock time equation (3.36) gives an R^2 of .985. Here the data included is for baseband S/N > 35 db. The high S/N model, $\hat{T}'_{ah}$ is

$$\begin{aligned} \hat{T}'_{ah} = [&B_1 + B_2 f(\xi) + B_3 |\Delta f'| + B_4 f^2(\xi) + B_5 |\Delta f'| \, f(\xi) \\ &+ B_6 |\Delta f'|^2 + B_7 |\Delta f'|^2 \, f(\xi) + B_8 |\Delta f'|^3 f(\xi) \\ &+ B_9 |\Delta f'|^4 + B_{10} |\Delta f'|^3] N^2, \end{aligned} \tag{5.7}$$

where

$$f(\xi) = \pi^2 (1 + 4\xi^2)^3 / 32\xi^4 \ . \tag{5.8}$$

The prime indicates normalization with respect to B_L. The values of B_i are given in Table 5.1.

The theoretical result, equation (3.36), corresponds to the B_7 term in (5.7). The value of $B_7 = .1784026$ compares favorably with $K_1 = .149$.

The linear terms in $\Delta f'$, B_3 and B_5 and the constant terms, B_1 and

Table 5.1

High S/N B_i for i = 1 to 10

i	B_i
1	136.2357
2	- 4.746776
3	- 5.348066
4	.03686420
5	- .1380053
6	2.494088
7	.1784026
8	- .006256406
9	- .008781083
10	- .2359511

B_2 improve the experimental model for small $|\Delta f'|/N$.

The data for large $|\Delta f'|/N$ appears to depart from a quadratic dependence upon $|\Delta f'|$ and approaches a linear dependence on $|\Delta f'|$ again. There does not appear to be a theoretical reason for this change but it seems to be a limitation caused by drift of the voltages and components in the experimental system. This effect is included in the regression model by the third and fourth order terms of $|\Delta f'|$. This effect could be included in a more accurate way by dividing the above model by a first order polynominal in $|\Delta f'|/N$. This was not done since WRAP is only applicable to models that are linear in B_i. NONLIN is applicable to any continuous non-linear model and could be applied here but this effect is parasitic and therefore not of theoretical importance. The investigation along this line was not carried further.

After trying several models for the general S/N case it was determined that the acquisition time dependence on the S/N is best approximated by an exponential function. NONLIN is used to obtain an optimum

set of parameter values for the exponential model. The model is

$$\hat{T}'_a = \hat{T}'_{ah}\ \mathrm{Exp}\{(N/S[B_{11} + |\Delta f'|^{.5}\ (B_{12} + B_{19}N^{.5} + B_{20}N + B_{21}|f''_c| + B_{22}\xi) + B_{13}|\Delta f'| + B_{23}\Delta f' f''_c + N^{.5}(B_{14} + B_{24}|f''_c|^{.5} + B_{25}|f''_c| + B_{26}\xi) + N(B_{15} + B_{27}|f''_c|^{.5} + B_{28}|f_c| + B_{29}\xi) + |f''_c|^{.5}(B_{16} + B_{30}\xi) + |f''_c|(B_{17} + B_{31}\xi) + B_{18}\xi + (N/S)^2[B_{32} + B_{33}|\Delta f'|^{.5} + B_{34}|\Delta f'| + B_{35}N^{.5} + B_{36}N + B_{37}|f''_c|^{.5} + B_{38}|f''_c| + B_{39}\xi]\} \qquad (5.9)$$

where

$$f''_c = [f_c - f_0]/B_L \qquad (5.10)$$

The optimum set of B_i, i = 1, $\cdots$, 39 is given in Table 5.2. It is noted that the values of B_i, i = 1, $\cdots$, 10 are only slightly different from those given in Table 5.1. This model results in an R^2 of .988.

It should be emphasized that the low S/N model is emperically derived and that additional data will probably give much greater insight as to the exact nature of the low S/N acquisition time dependence on f'_c, Δf ξ, B_L, N and S/N. An examination of the residuals based on this model indicates that the fit for most of the data is quite good. There are cases for which the fit is poor. These are for large $|f''_c|$ and large N. There are also several values of $\Delta f'$ for which the fit is poor. These are - 1.33, 2.67 and $\Delta f' \geq$ - 7.8. There does not seem to be a general trend since for $\Delta f'$ = - 2.67 the fit is good.

For f'_c = - .25, it appears that the model is poor. For this case the initial and final frequencies are on symetrically opposite sides of the input noise spectrum. For the other data, both points are on the

Table 5.2

Final B_i for i = 1 to 39

i	B_i
1	139.325458
2	- 4.8543155
3	- 5.78910118
4	.0376510209
5	- .131120192
6	2.75745172
7	.174072319
8	- .00555608252
9	.00961498892
10	- .291347655
11	-250.102571
12	116.432715
13	- 8.39448372
14	136.780342
15	- 29.5281854
16	- 63.6606611
17	11.0358370
18	71.858413
19	1.17281344
20	.0479439337
21	.0216635654
22	- 30.8514584
23	.00476079058
24	1.56316733
25	- 3.24723681
26	- 42.7491549
27	- 1.21578248
28	.750814398
29	9.77283735
30	37.3890090
31	- 4.68228870
32	1809.18859
33	331.694756
34	86.9580755
35	-2538.86699
36	186.766918
37	34.9421937
38	- 5.31458145
39	837.582137

same side of the spectrum. It appears that the former condition tends to complicate the model.

It is believed that the model would have been easier to obtain and interpret if fewer parameters had been investigated. That is, if the data had been restricted to the case of $f_c'' = 0$, $\xi = 1$ and $B_L = 75$. By considering more points of Δf, S/N and N, and a more uniform selection of points in this space, it would have been possible to obtain a more meaningful and accurate model.

It is possible to give a few rules of thumb concerning the low S/N acquisition time. In general the data indicates that the acquisition time has an exponential dependence upon the N/S level. For all cases considered it is conservative to say that

$$\hat{T}_a' = \hat{T}_{ah}' \text{ Exp}[1800 \text{ N/S}]. \qquad (5.11)$$

VI. EXPERIMENTAL THRESHOLD

The FM threshold experiment for the ELRPLL is described and the results are presented in this chapter. A few general conclusions are made.

In view of the difficulties experienced by other authors in attempting to obtain a theoretical model for the PLL threshold it seems desirable that an experimental investigation of the ELRPLL threshold be conducted.

The first problem is the selection of a threshold criteria. Then an experiment is designed to determine conditions for which the criteria is satisfied. An experimental system is designed and implemented. After these preliminaries data is taken using the experimental model. This data is analysed to determine when the threshold criteria is satisfied.

This chapter selects a threshold criteria, describes an experimental procedure to determine threshold along with the experimental system and presents data in graphical form taken using this experimental procedure. This is done for a class of signal and ELRPLL parameter values. The class includes several values of sinusoidal modulation frequency, ELRPLL damping and N. For comparison, data is taken for a first order ELRPLL and for a PLL with a sinusoidal phase detector. A set of plots is also obtained for various N and modulation bandwidths for the case of band-limited white, gaussian, random modulation.

6.1. Criteria for Threshold

Chapter II discusses in some detail the various definitions that are used as a criteria for the FM improvement threshold. Threshold is defined in this study as the minimum input S/N level referred to the output band for which there exists a value of the modulation index for a given output S/N level. The appropriateness of this definition appears when one considers a typical input/output S/N plot of an FM demodulator for a class of modulation indexes. In general this family of curves defines the boundary of a forbidden region similar to that which Develet [6] gives in his Figure 4 for the PLL threshold and Shannon's limit. This definition was selected because it seemed to provide the best combination of the qualities of measurability and relevance to the intuitive notion of intelligibility of the demodulator output. It is easily used for various modulation spectra.

6.2. Threshold Experiment

There are at least two procedures that can be used to determine the FM threshold of the ELRPLL using the above definition. The first, which is not used, is to measure the output S/N versus input S/N level and adjust the modulation index so that for a given level of output S/N the input S/N referred to the output band is minimized. The second, which is used, is to measure and plot the output S/N as a function of the input S/N for a class of modulation indexes. This procedure has been used traditionally to demonstrate graphically the departure of the output S/N from a linear dependence upon the input S/N. When each family of input/output (I/O) S/N curves is completed the threshold level is defined by a curved line drawn tangent to the upper left corner of each curve of the

family. This procedure was chosen in preference to the first because it provides more than just the threshold information. It gives I/O S/N data.

The ELRPLL system described in Chapter IV and Appendix B is used to determine the I/O S/N plots. This experiment has two parts. Part one is for sinusoidal modulation and part two is for bandlimited, white, gaussian, random modulation. They are considered in that order. These two choices are made because it is felt that they represent two extremes of the various types of modulation waveforms. The first is the most deterministic and simplest of all the non-trivial types of modulation and the second represents the most undeterministic and complex of all the practical types of modulation. It is intuitively felt that these two extremes give a better feeling for the upper and lower bounds of the threshold dependence upon modulation spectrum than any other pair of choices.

6.2.1. Sinusoidal Modulation

The experimental FM threshold of the ELRPLL for the case of sinusoidal frequency modulated carrier with additive, bandlimited, gaussian, noise is considered in this section. Figure 6.1 is a block diagram of the test set up used to measure the I/O S/N data.

The sinusoidal modulation is generated by the HP 200CD signal generator. The modulation index is set by the HP 350D attenuator. The GR 1390B noise generator generates the random signal necessary for the additive channel noise. The input S/N level is set by the second HP 350D attenuator. The frequency modulated carrier is added to the random signal and the sum is filtered by the channel filter. This filter has a

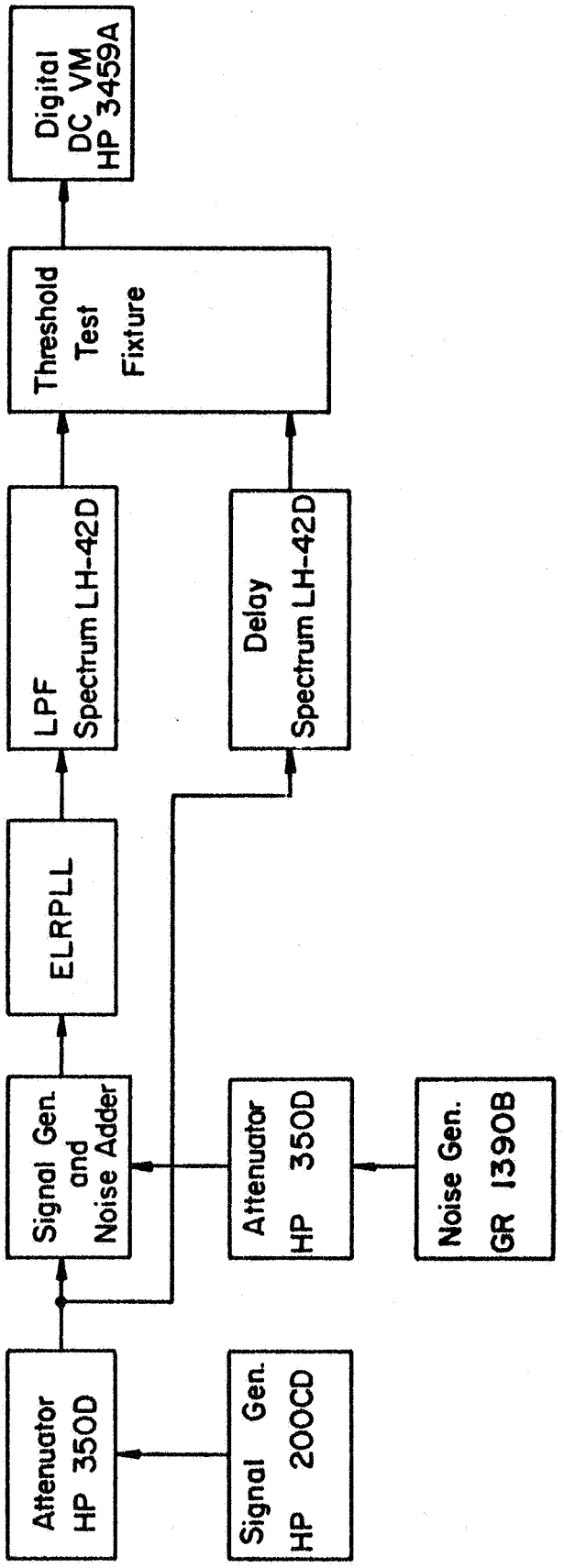

FIGURE 6.1. THRESHOLD TEST SET UP FOR SINUSOIDAL MODULATION.

linear 7 pole butterworth response. The 3 db bandwidth is 10 KHz. and the center frequency is 100 KHz. This approximates the IF response of most receiving systems where a high level of adjacent channel rejection is desired and little frequency distortion in the pass band can be tolerated. Appendix C gives more detailed information concerning the Signal Generator and Noise Adder.

The output of the simulated IF drives the ELRPLL. The loop filter output of the ELRPLL drives the LH-42D LPF. This filter has a 7 pole butterworth low pass linear response. The 3 db cutoff frequency is adjusted to the frequency of the modulation as is usually done. The modulation is also delayed in the second LH-42D by an amount of time equal to the delay of the channel and demodulator.

The delayed modulation replica and the demodulator output are combined in the Threshold Test Fixture. Appendix E gives a detailed description of the Threshold Test Fixture and its principles of operation. This fixture operates on the two inputs and uses a multiplier to provide real time mean square estimates of the signal power, the signal plus noise power and the noise power. These are measured by the Digital DCVM.

The data obtained in this manner is computer processed to correct for known measurement biases, such as meter loading of the circuits and non-ideally bandlimited channel noise spectrum. For further details see Appendix E. From the corrected data an estimate of the output S/N level in the output band is calculated. This data is plotted in Figures 6.2 through 6.14. In each figure the I/O S/N referred to the output band is plotted for several values of the RMS modulation index. The RMS modulation index is defined as the RMS frequency deviation divided by the modulation frequency or bandwidth. This is done to facilitate a

comparison of the threshold results for the sinusoidal modulation case with those for the random modulation case. On all the I/O S/N curves the modulation index is labeled in db and in ratio. In each case the number in parentheses is the ratio. Here db is understood to be 20 log of the ratio. The term β is the modulation index.

Throughout this study the modulation frequency has been normalized. This is done by dividing the modulation frequency or bandwidth by the bandwidth of the ELRPLL.

The output noise is determined by subtracting the output signal power from the output power. For the high S/N case the quantities are nearly equal. Therefore the accuracy of the calculated noise power is a decreasing function of the output S/N level. The measurements are only accurate to 2 significant figures for the high S/N case. Therefore the output S/N level calculation is poor above an output S/N of 10 db and is useless above 20 db. Data is only considered when the output S/N is less than 20 db. The high S/N curves are obtained by determining the high S/N theoretical FM asymptotes. Each composite curve is based on a combination of both the data points indicated on the plots and these asymptotes.

Figures 6.2 through 6.5 are the I/O S/N curves of the second order ELRPLL for a modulation frequency of .133, damping ratio of 1 and for values of N = 1, 2, 8, and 32 respectively. In the first two cases the maximum modulation index is limited by the cycle slipping of the ELRPLL. In the latter two this is not the case. The effect of the cycle slipping due to modulation causes the horizontal displacement of the curves in the neighborhood of 10 db output S/N level. At high modulation index

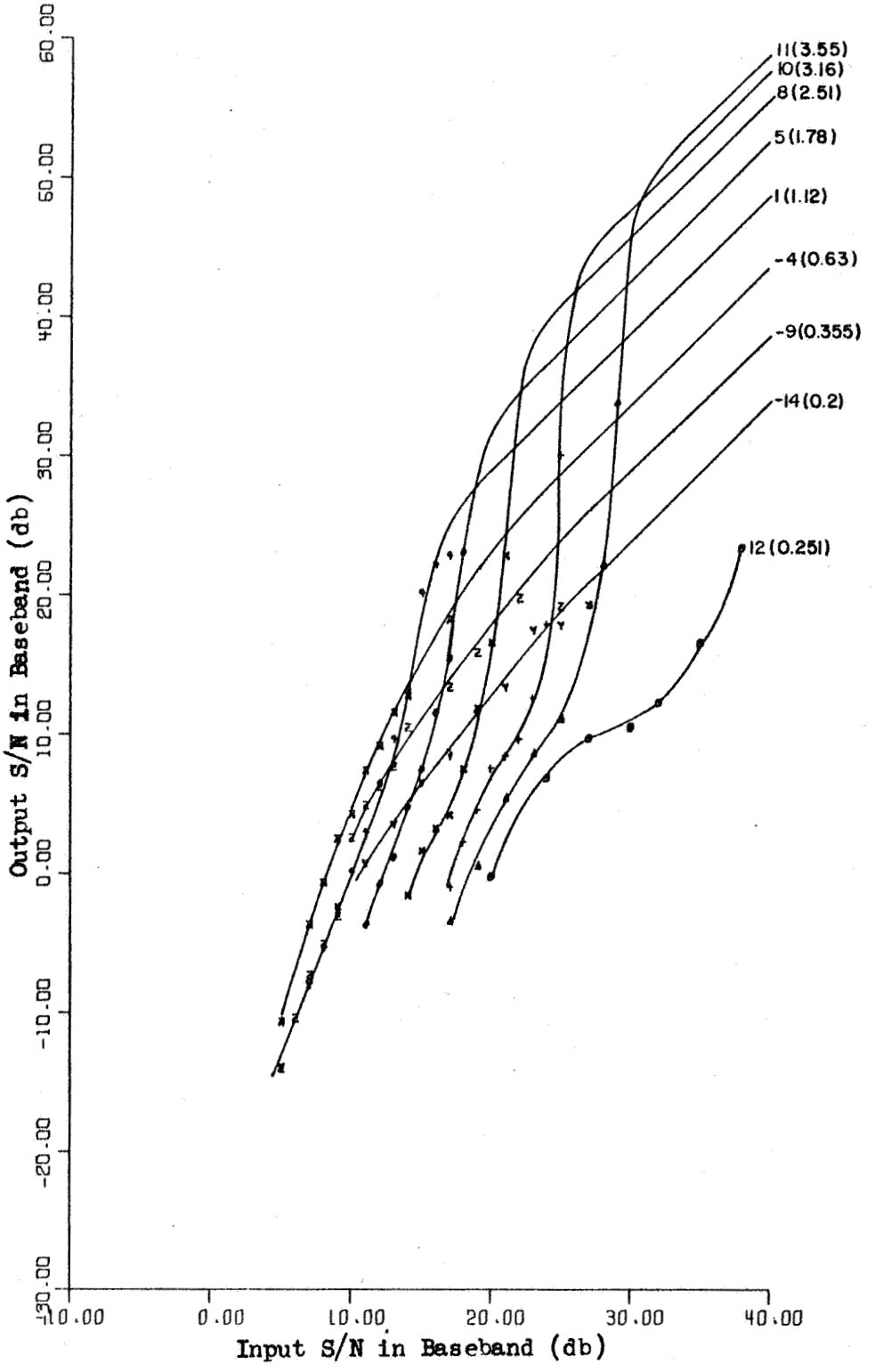

Figure 6.2. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = 1 and N = 1

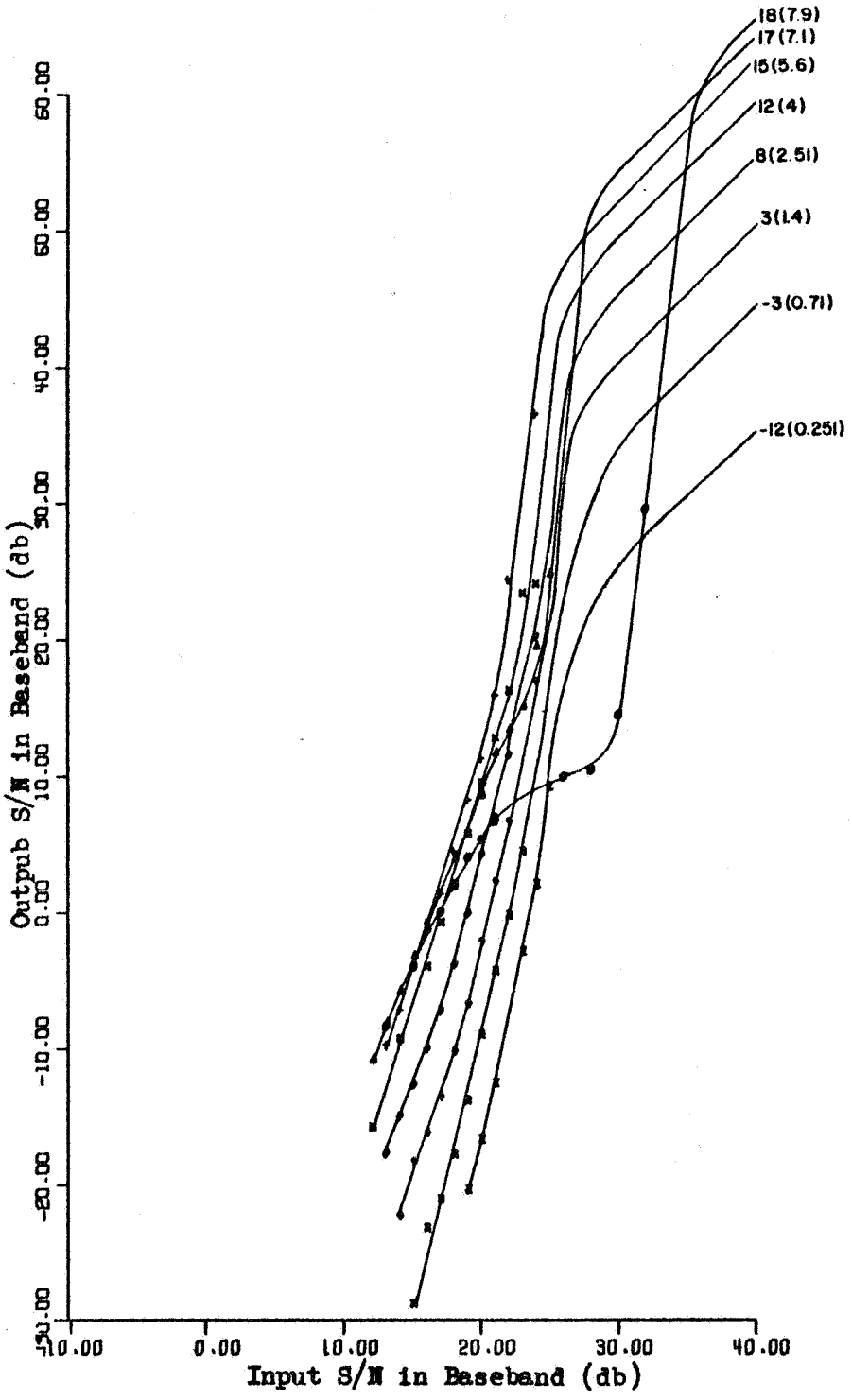

Figure 6.3. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = 1 and N = 2

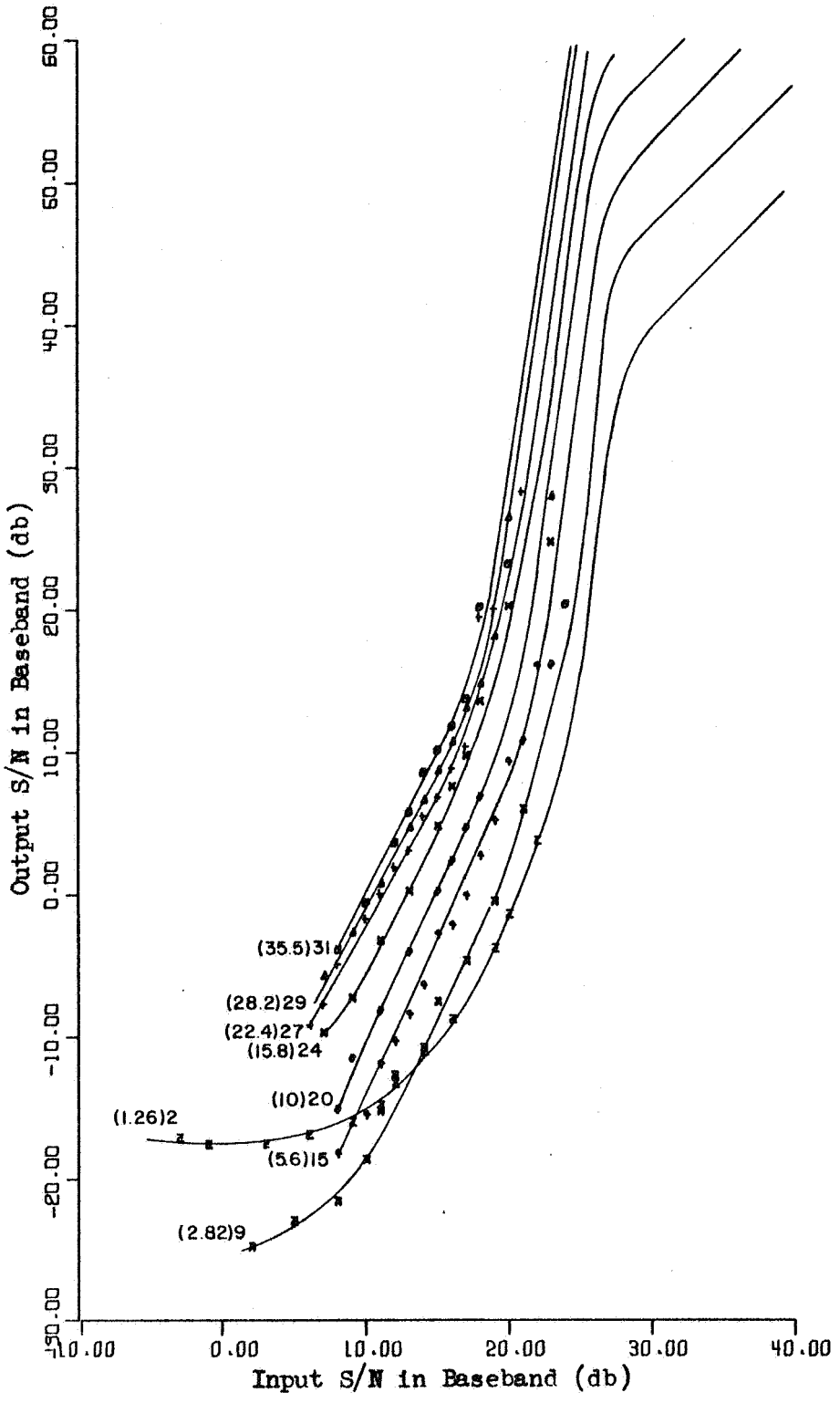

Figure 6.4. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = 1 and N = 8

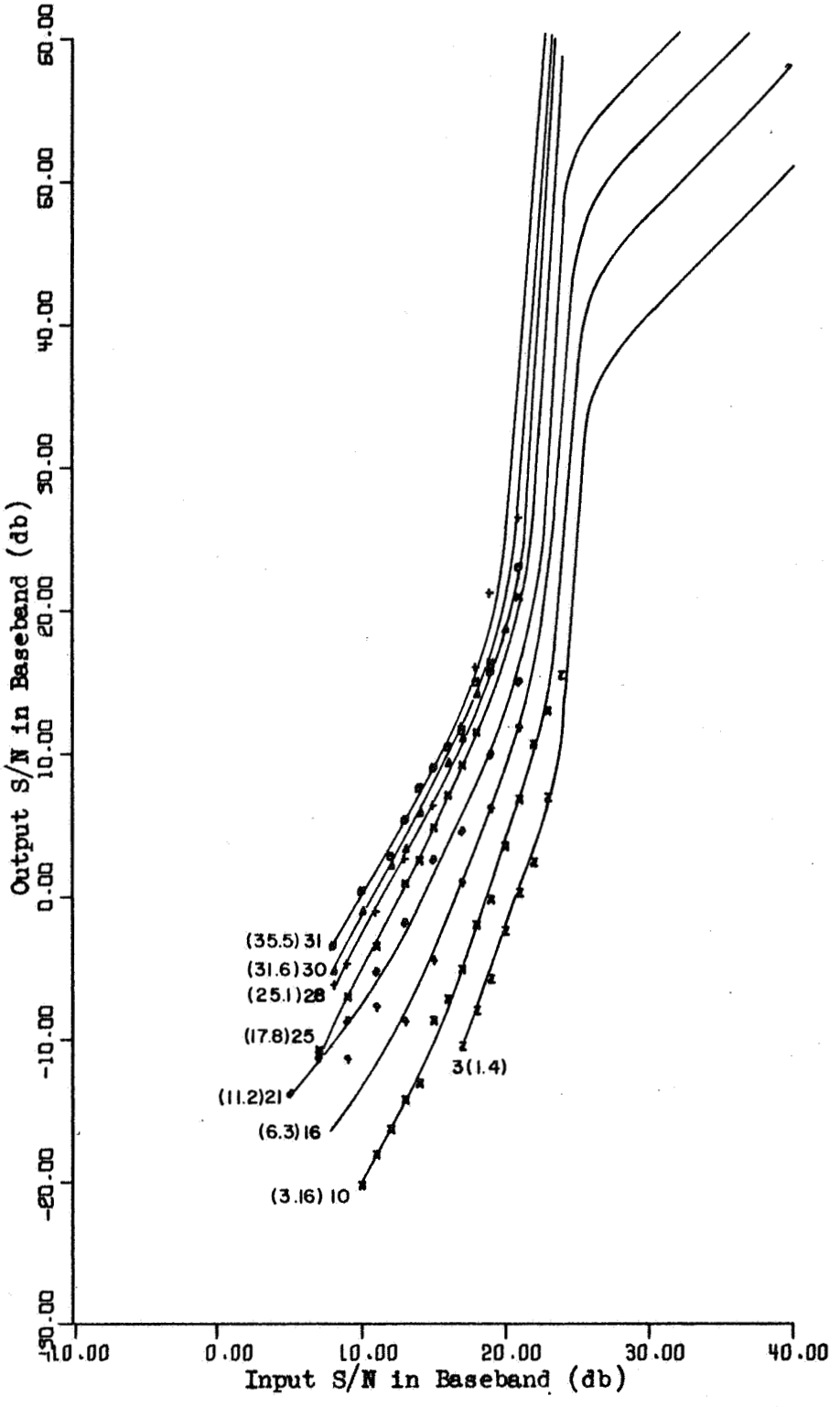

Figure 6.5. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = 1 and N = 32

the modulation alone will cause cycle slipping. In Figures 6.2 and 6.3 the highest index used is the maximum value that will not cause cycle slipping. Here only a very small amount of noise is needed to cause cycle slips during modulation peaks. These cycle slips cause distortion and hence suppression of the output signal and the discontinuities generated as a result cause the output noise to increase rapidly with a slight decrease in the input S/N level. Because of this the curves in Figure 6.2 for $\beta \geq 8$ db have a left shift for increasing input S/N near the output level of 10 db and appear to have steeper slopes to the right of this shift. A similar phenomenon is apparent in Figure 6.3 for $\beta \geq 17$ db and in several other figures.

Figure 6.6 is a comparison of the threshold curves obtained from Figures 6.2 through 6.5. Each threshold line is obtained by constructing a curved line tangent to the threshold break point of the curve for each value of modulation index. This is done since it is not possible to obtain I/O data for a continuous class of β. Therefore the threshold curves are approximated between tangencies by a smooth curved line drawn so that the tangent line and its derivative are continuous. Figure 6.6 is a comparison of the threshold curves for several values of N for $f_m' = .133$ and $\xi = 1$. It is noted that the case of N = 0 is for a PLL with a sinusoidal phase detector characteristic. This data is obtained from Figure 6.18 and is included here for comparison.

Note that for input S/N < 14 db, N = 0 gives the lowest threshold. For input S/N > 21 db N = 32 gives the lowest threshold of the class of N considered. Between these two levels of input S/N, N = 1 is optimum.

For input S/N < 22 db, N = 2 yields the highest threshold. It is

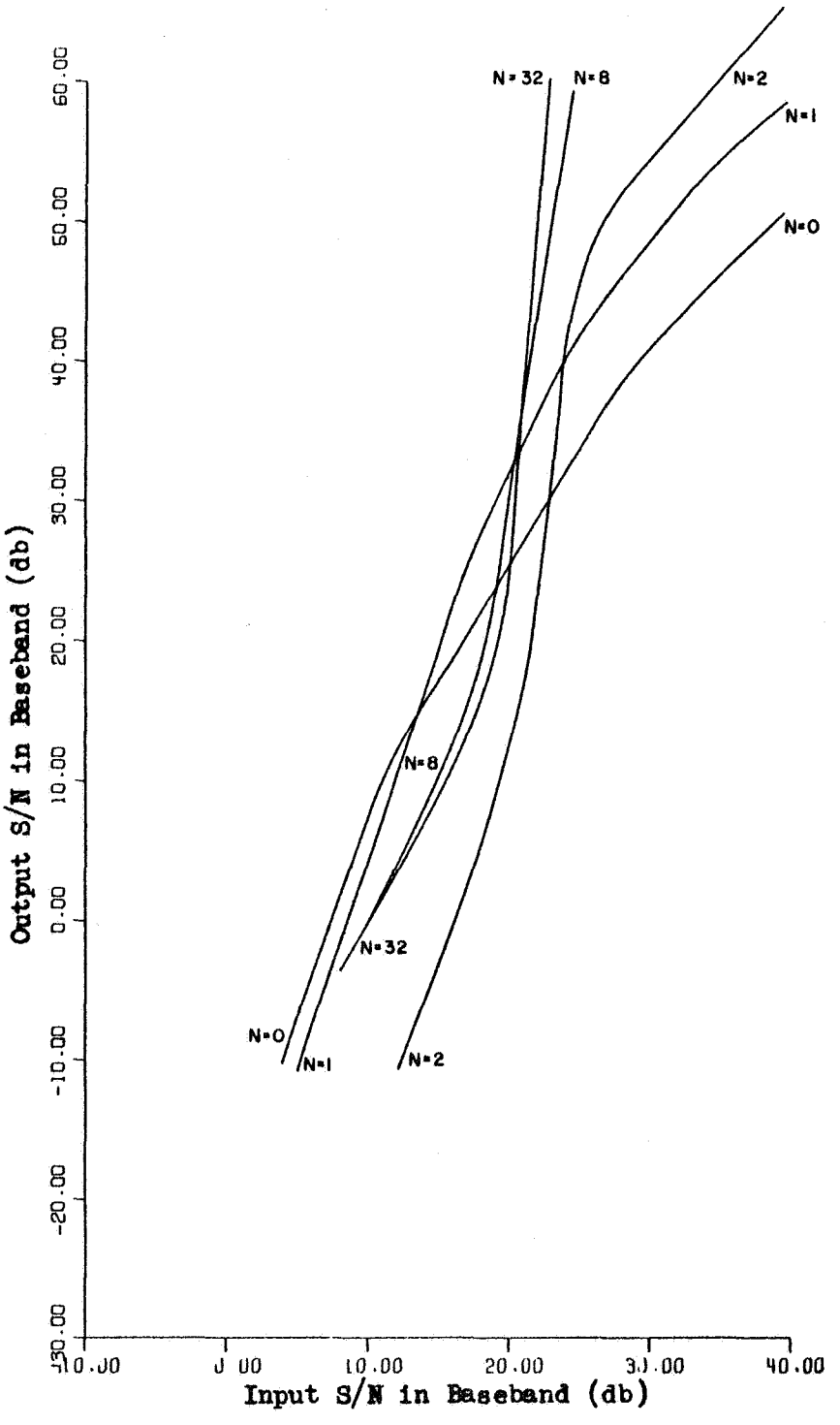

Figure 6.6. FM Threshold Curves for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133 for Several Values of M

not understood why this occurs since for Figure 6.16 the threshold level is monotonic in N at the high and low S/N ends of the curves.

For sufficiently high modulation index, the threshold line is determined by the modulation. Therefore the threshold lines theoretically approach an angle of 45°. This is clearly seen to occur for N = 0, 1 and 2. However this portion of the curves for $N \geq 8$ is off the graph and is not shown.

When the input S/N level is greater than 21 db the threshold of the ELRPLL for $N \geq 8$ is at least 4 db greater than that of a PLL. When the input S/N level is greater than 22 db and $N \geq 8$ the threshold improvement is greater than 15 db.

Figures 6.7 and 6.8 are the I/O S/N curves for the case where N is 1, modulation frequency is .133 and damping ratio is .5 and 2 respectively. Here the maximum modulation index in both cases is limited by cycle slipping. This causes a horizontal offset similar to that in Figures 6.2 and 6.3.

The threshold of the ELRPLL for $f_m' = .133$, N = 1 and several values of ξ are compared in Figure 6.9. This data is obtained from Figures 6.2, 6.7, 6.8 and 6.14. The case of $\xi = \infty$ is for a first order ELRPLL.

The threshold is lowest for the first order ELRPLL except for input S/N levels in the neighborhood of 20 db. In this region it is concluded that for $\xi \geq 1$, ξ has no effect upon the threshold since the curves are so close together. Outside this region the threshold is a monotonic function of ξ.

Figures 6.10 through 6.12 are the I/O S/N curves for the ELRPLL for the case of N = 1, ξ = 1 and modulation frequencies of .267, .067, and

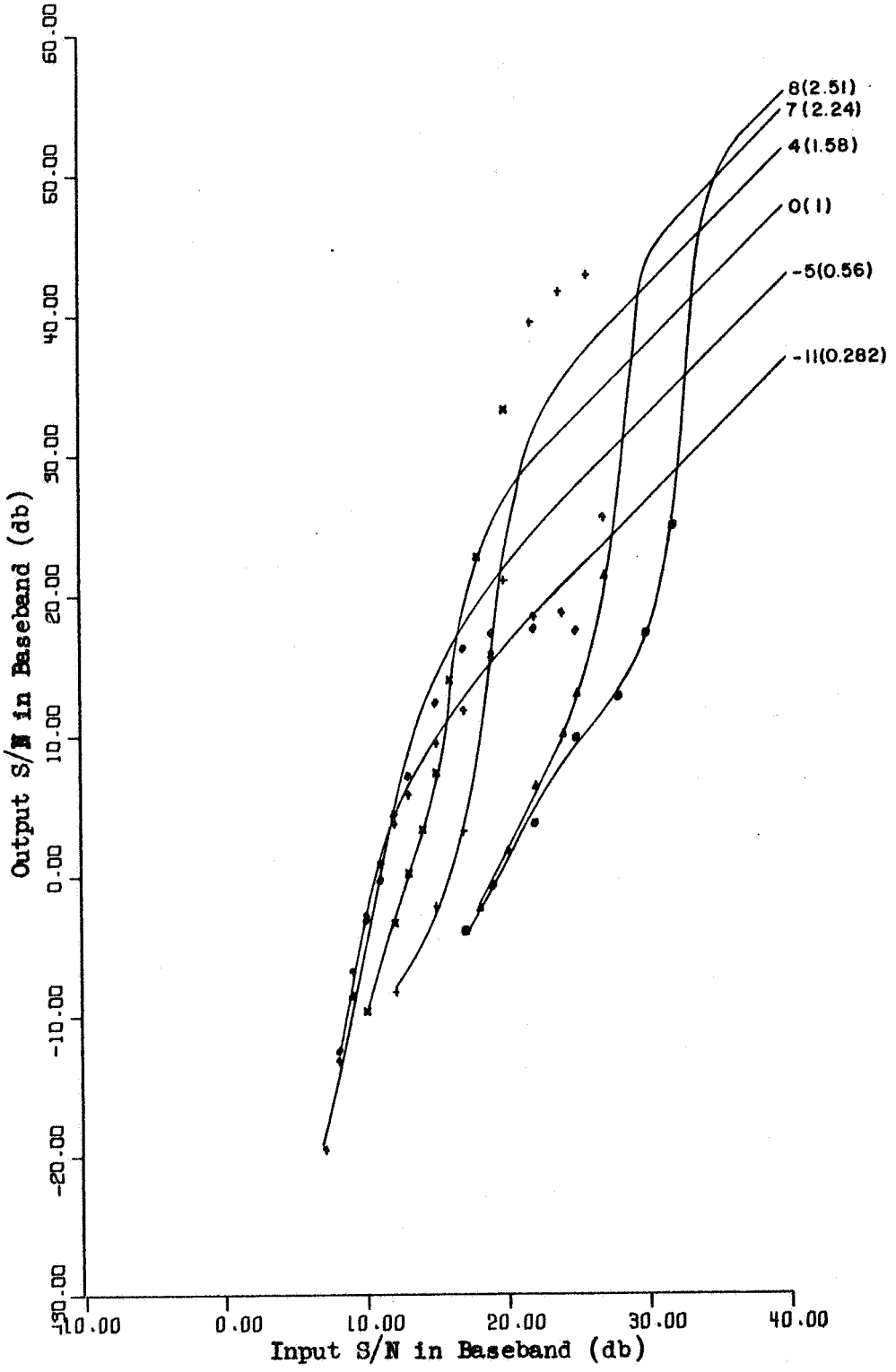

Figure 6.7 Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = .5 and N = 1

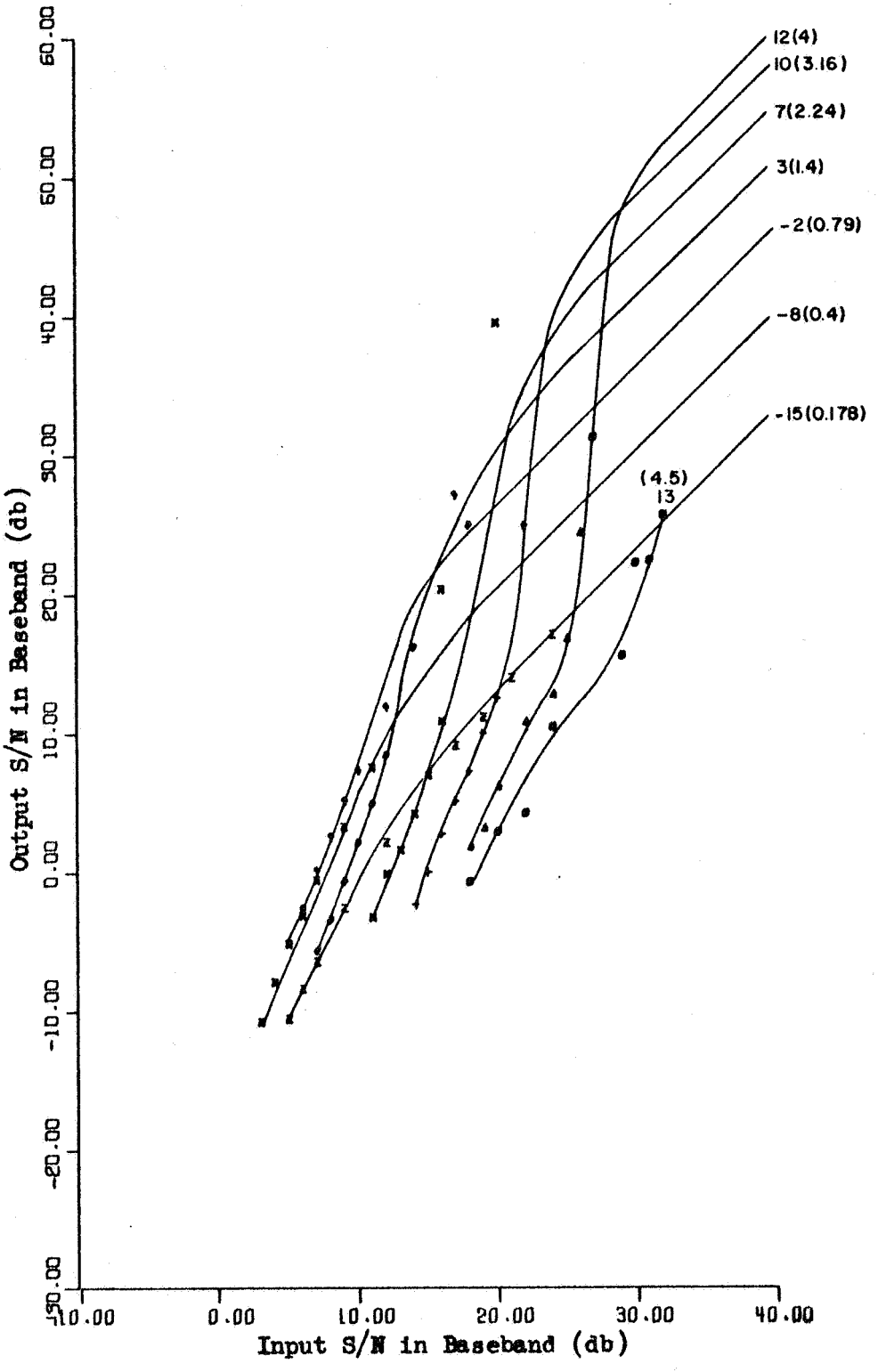

Figure 6.8. Input/Output S/N (Baseband) for a second Order ELRPLL with Sinusoidal Modulation Frequency = .133, Damping Ratio = 2 and N = 1

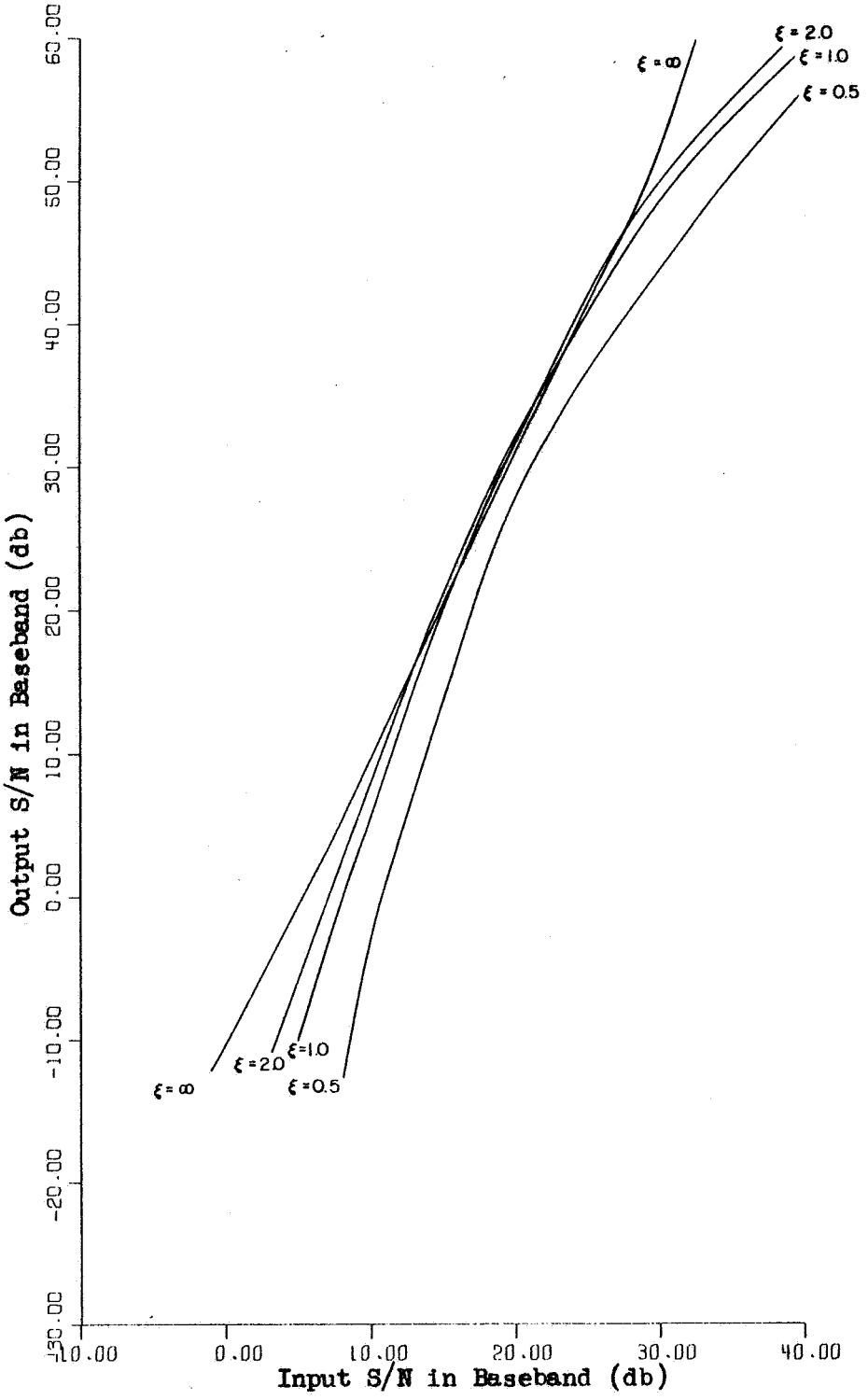

Figure 6.9. FM Threshold Curves for a First and Second Order ELRPLL with Sinusoidal Modulation Frequency = .133 and N = 1 for Several Damping Ratios

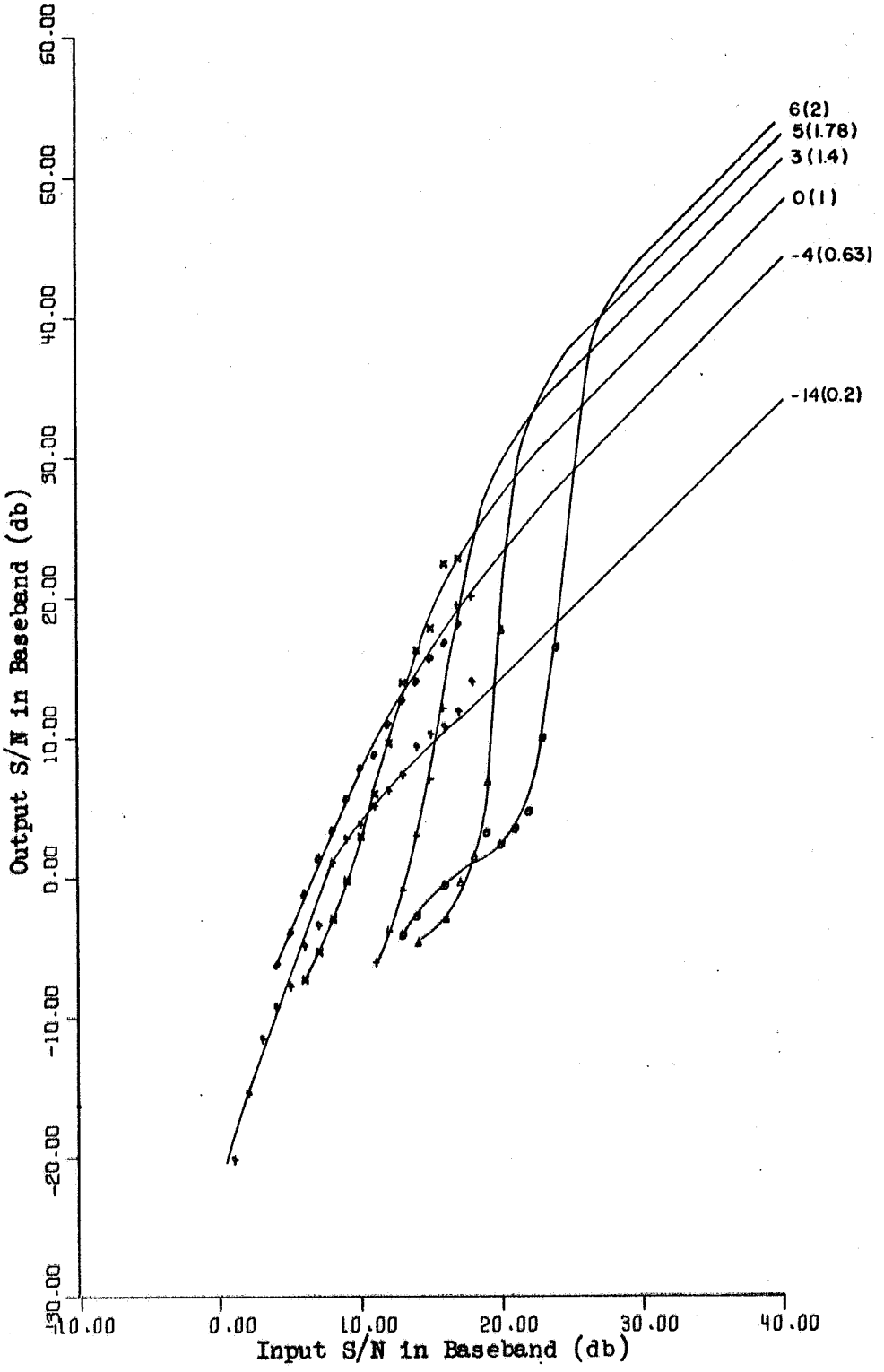

Figure 6.10. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .267, Damping Ratio = 1 and N = 1

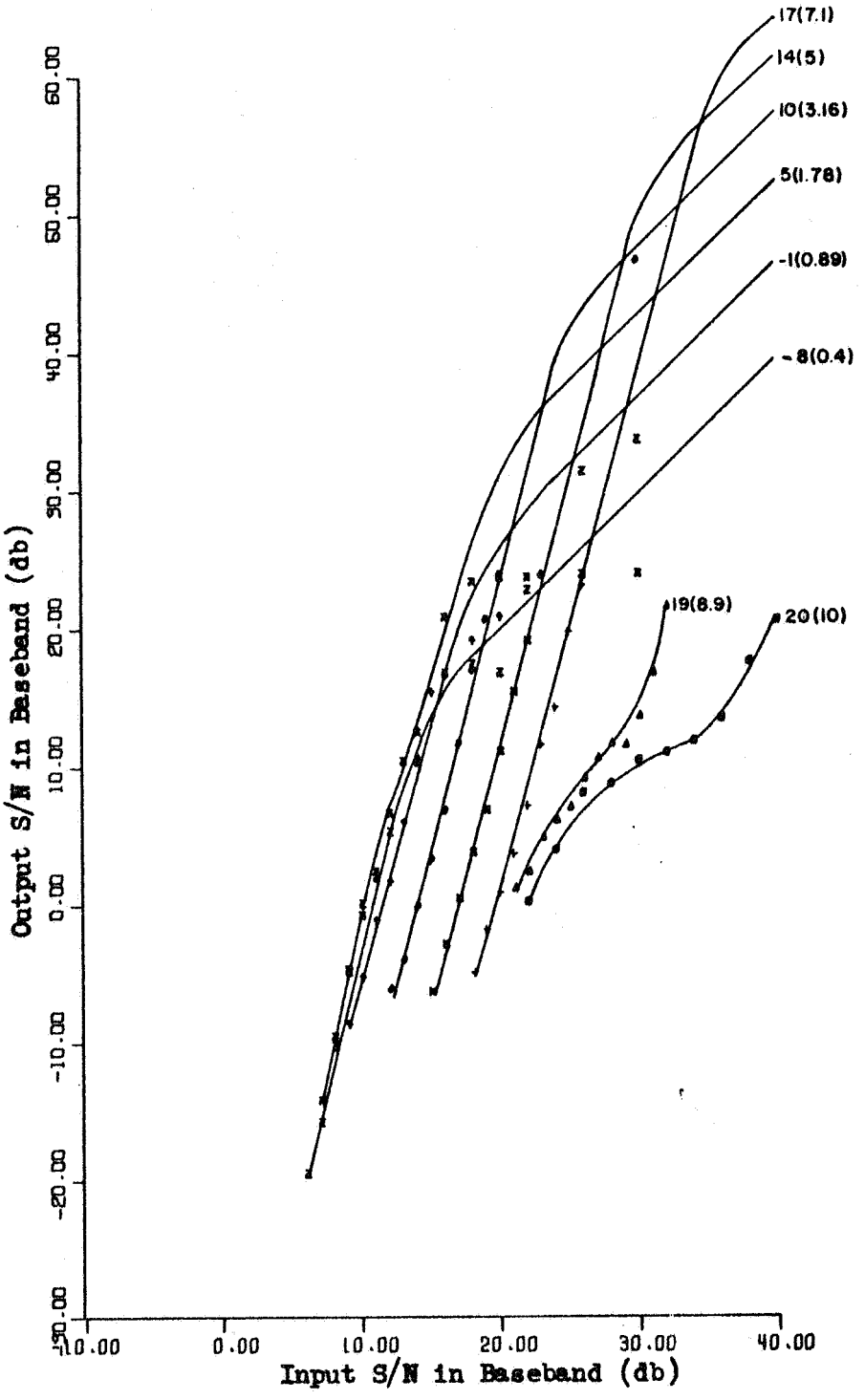

Figure 6.11. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .067, Damping Ratio = 1 and N = 1

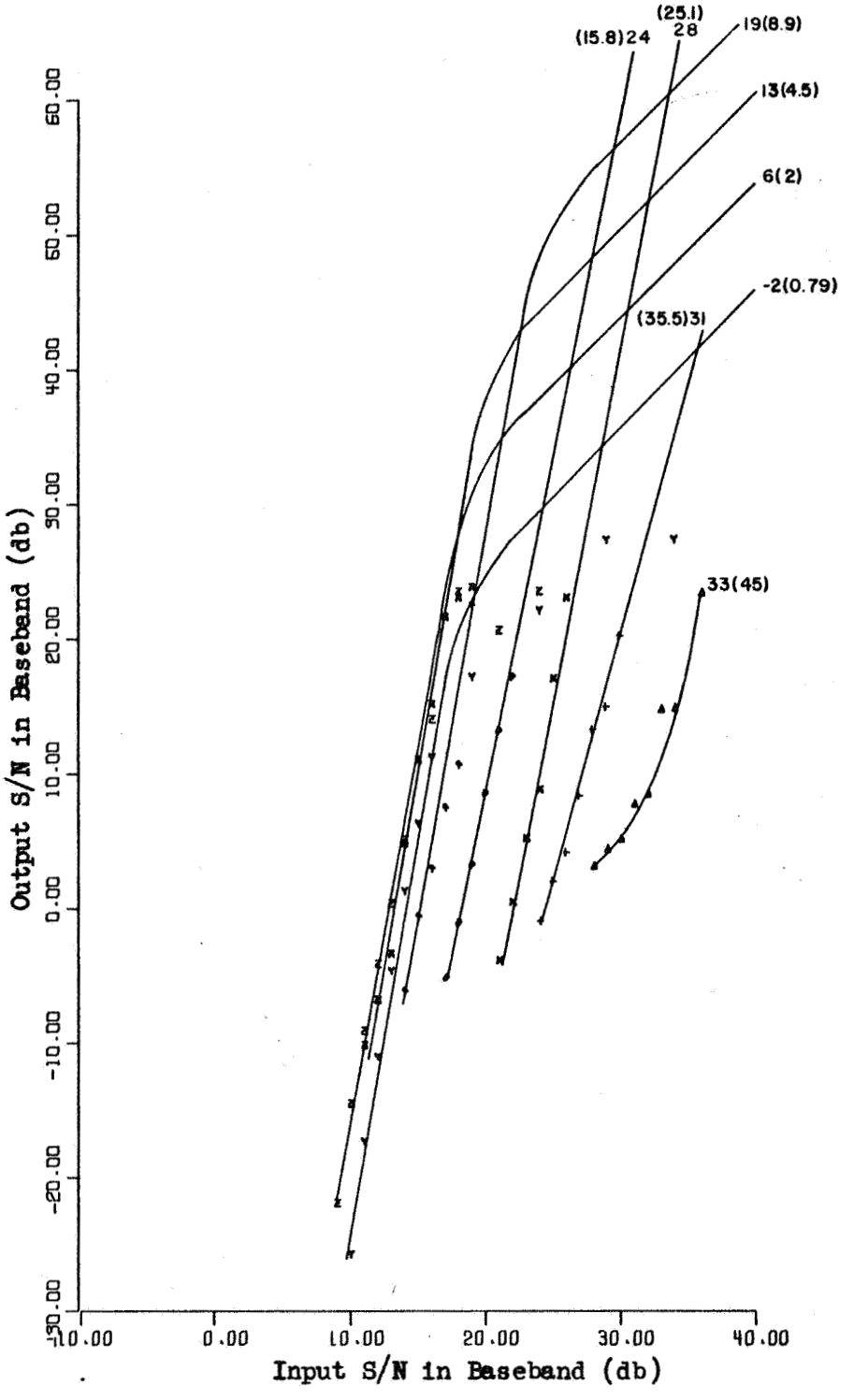

Figure 6.12. Input/Output S/N (Baseband) for a Second Order ELRPLL with Sinusoidal Modulation Frequency = .027, Damping Ratio = 1 and N = 1

.027 respectively. For all three cases the maximum modulation index is limited by cycle slipping. In each of these cases the same horizontal offset of the curves as mentioned above is evident in the 0 to 10 db output S/N region.

The thresholds for the ELRPLL with N = 1, ξ = 1 and several values of f_m' are compared in Figure 6.13. This data is obtained from Figures 6.2, 6.10, 6.11 and 6.12.

The threshold is loweved for input S/N > 18 db by decreasing f_m' and for S/N < 18 by increasing f_m'. Since $f_m' = f_m/B_L$ the threshold can be reduced for high input S/N level by increasing the loop bandwidth.

Figures 6.14 and 6.15 are the I/O S/N curves of the first order ELRPLL for the case of .133 modulation frequency with N = 1 and 2 respectively. In both cases the same horizontal offset as mentioned is evident.

The thresholds for these cases are compared with that for the first order PLL with sinusoidal phase detector in Figure 6.16. The data for the latter case (N = 0) is obtained from Figure 6.17.

When the input S/N level is greater than 21 db the first order ELRPLL has a lower threshold than the PLL and the threshold is a monotonic function of N. Below this level the relationship is reversed and the PLL has the lowest threshold. However the threshold improvement of the PLL is less than 2 db worst case and that of the ELRPLL for input S/N > 25 db is better than 15 db.

In order to provide a meaningful means of comparing the threshold properties of the ELRPLL with those of a PLL having a sinusoidal

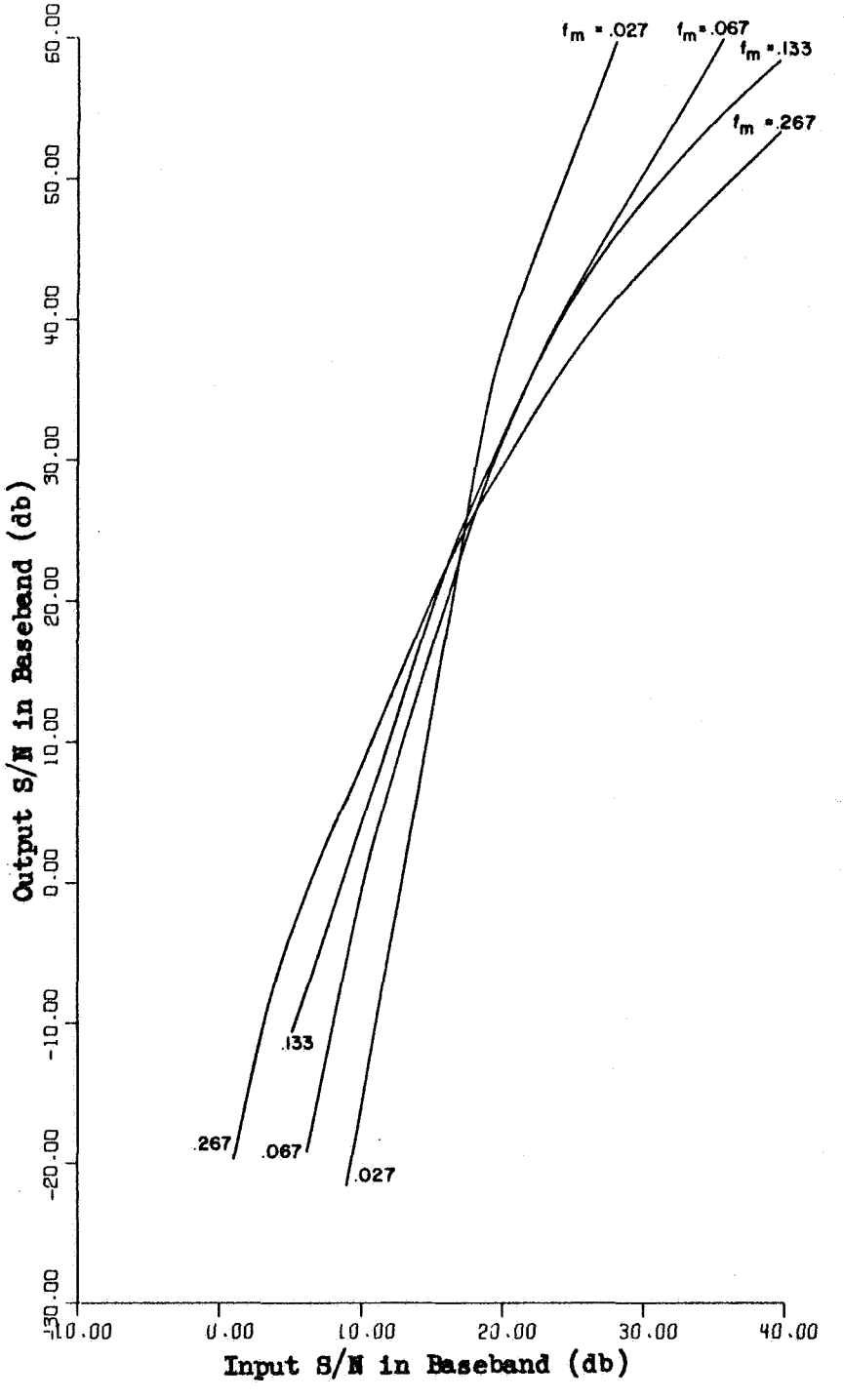

Figure 6.13. FM Threshold Curves for a Second Order ELRPLL with N = 1 and Damping Ratio = 1 for Several Sinusoidal Modulation Frequencies

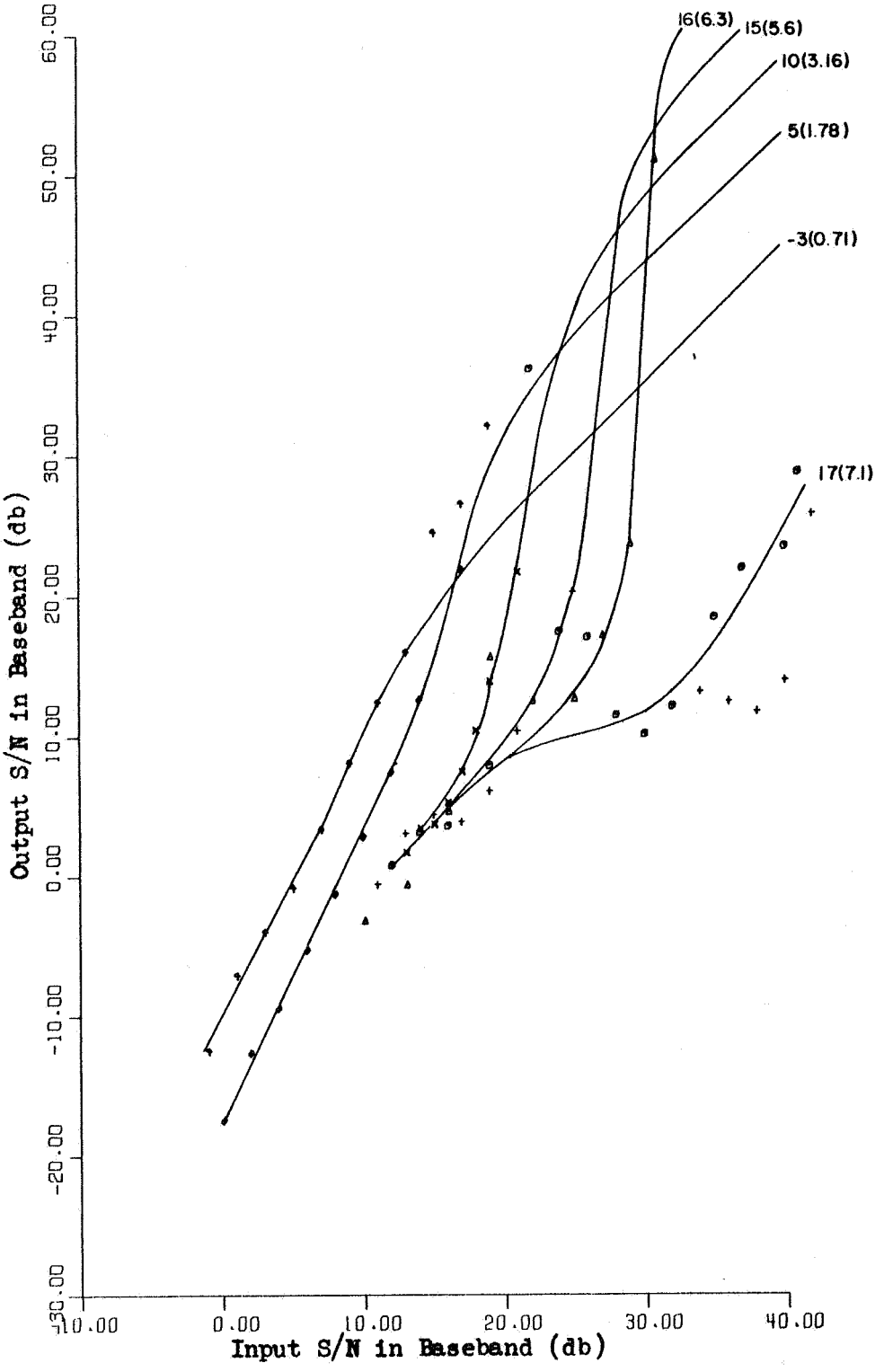

Figure 6.14. Input/Output S/N (Baseband) for a First Order ELRPLL with Sinusoidal Modulation Frequency = .133 and N = 1

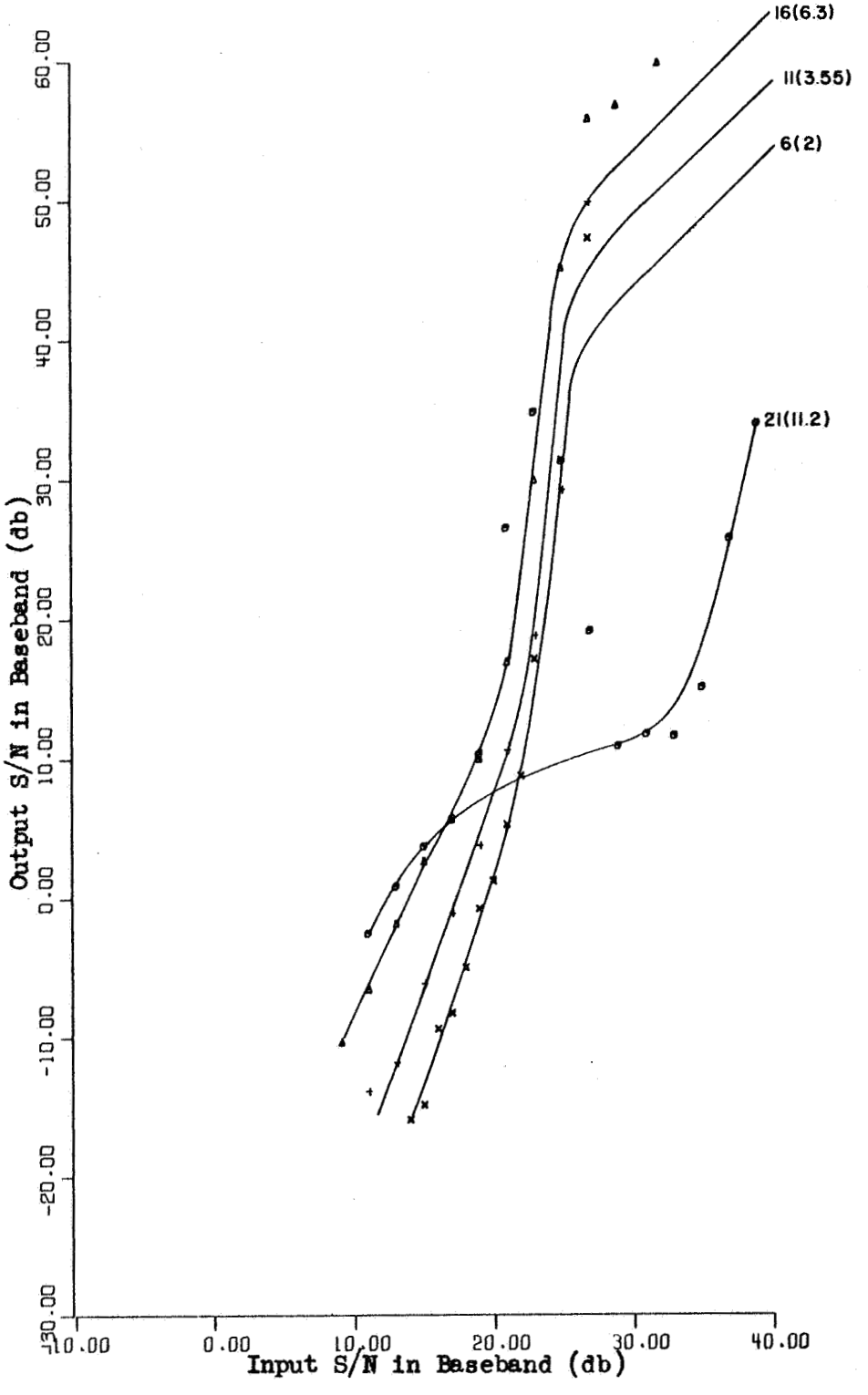

Figure 6.15. Input/Output S/N (Baseband) for a First Order ELRPLL with Sinusoidal Modulation Frequency = .133 and N = 2

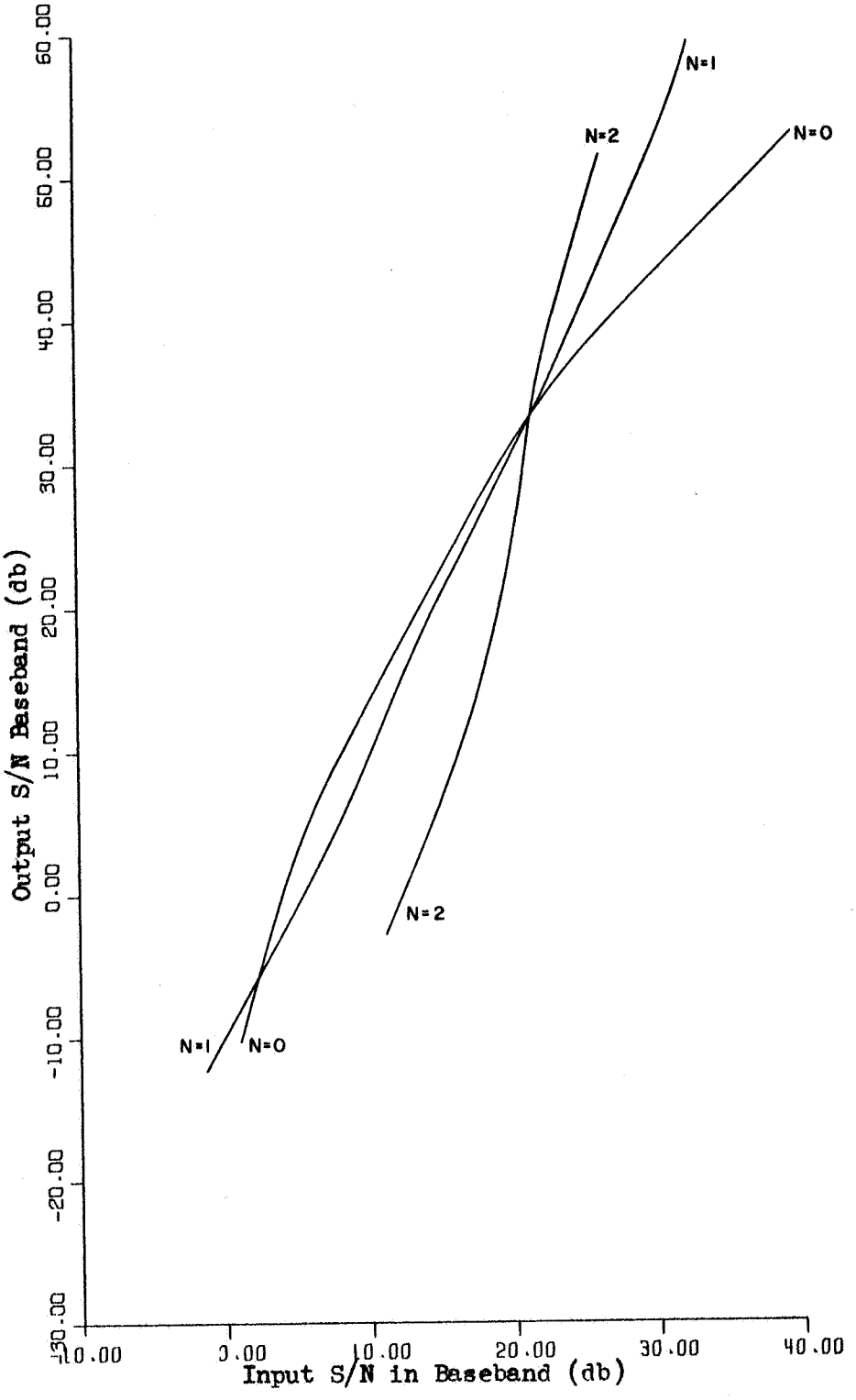

Figure 6.16. FM Threshold Curves for a First Order ELRPLL and a First Order PLL with a Sinusoidal Phase Detector Characteristic (N = 0) for Sinusoidal Modulation Frequency = .133

characteristic, a set of data is obtained for the latter system using the same equipment. The first order and second order loop with $\xi = 1$ are considered for the case of .133 modulation frequency. This data is presented in Figures 6.17 and 6.18 respectively. The threshold for the first order PLL and for the second order PLL with $\xi = 1$ are compared in Figure 6.19. It is apparent that the first order PLL has a 2 db lower threshold than the second order PLL with $\xi = 1$ for high S/N levels. It is also apparent that the first order PLL can demodulate a signal with a slightly higher modulation index. Comparing Figures 6.9 and 6.19 it is noted that the first order ELRPLL also has a slight threshold advantage at high input S/N levels.

In general it is concluded that for the case of sinusoidal modulation there are 2 mechanisms whereby one can exchange low input S/N threshold for high input S/N threshold. From Figures 6.6 and 6.16 it is clear that increasing N improves the high S/N threshold of the ELRPLL. From Figure 6.9 one sees that increasing B_L improves the high S/N threshold. A comparison of the three figures shows that for the cases considered the same improvement in threshold can be obtained by a 2 to 1 change in N or B_L. Since it is easier to increase B_L than N, the optimum FM demodulator of those considered is the ELRPLL with N = 1. Then one can optimize B_L for the lowest threshold for the input S/N range of interest.

6.2.2. Random Modulation

The experimental FM threshold of the ELRPLL for the case of bandlimited, white, gaussian, randomly modulated carrier with independent, additive, bandlimited, white, gaussian, channel noise is considered in

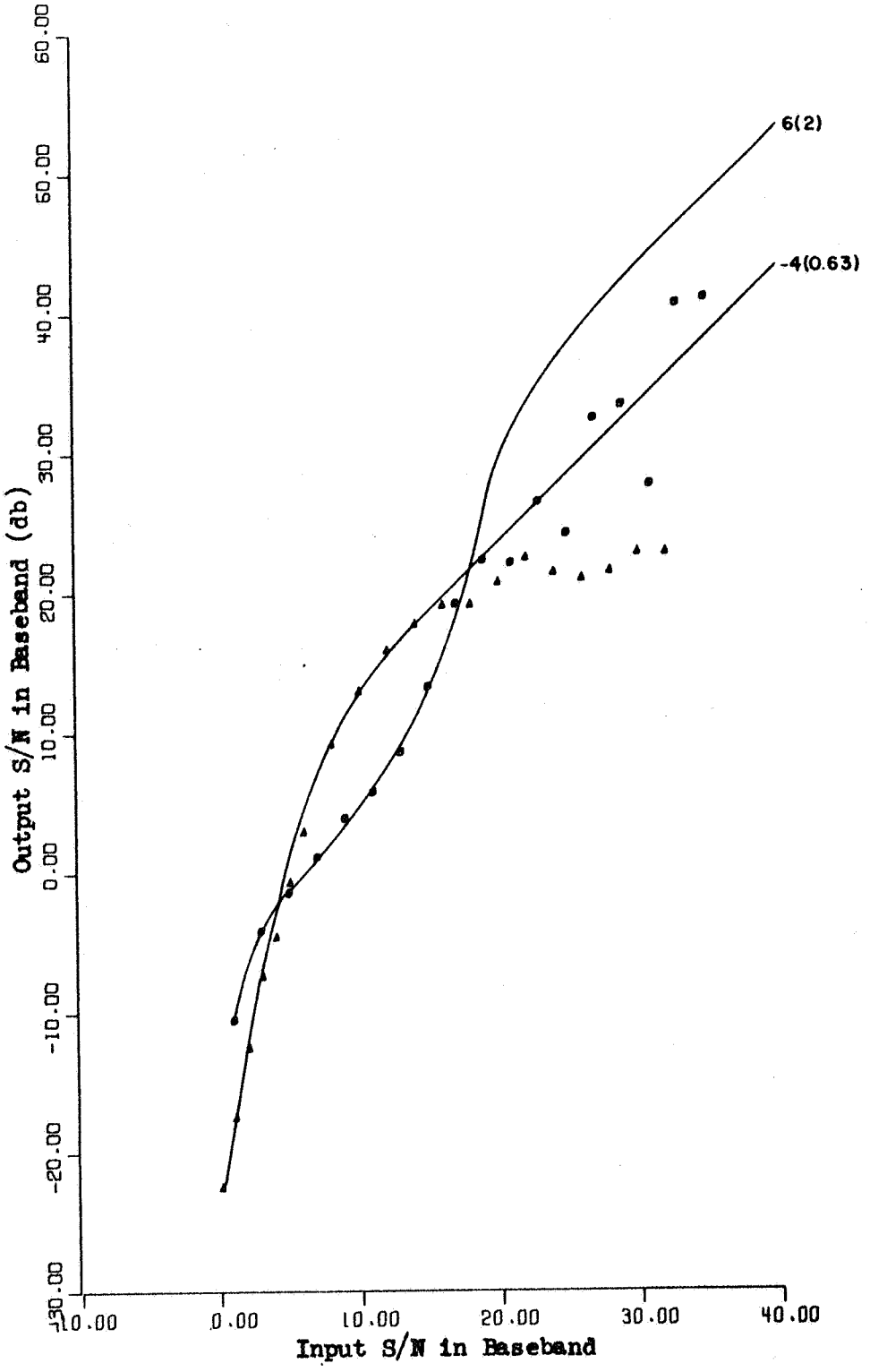

Figure 6.17. Input/Output S/N (Baseband) for a First Order PLL with Sinusoidal Phase Detector Characteristic and Modulation Frequency = .133

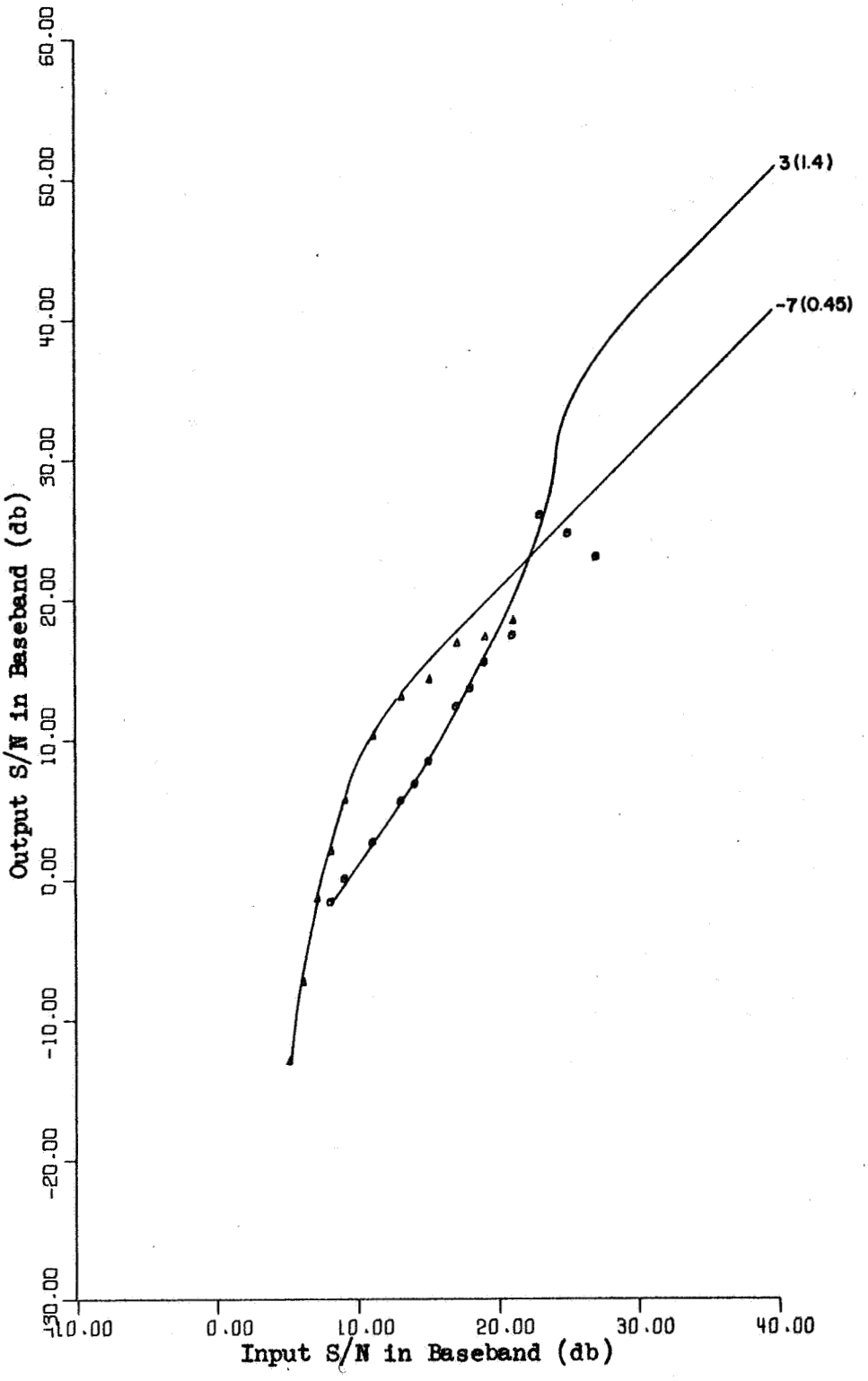

Figure 6.18. Input/Output S/N (Baseband) for a Second Order PLL with Sinusoidal Phase Detector Characteristic, Sinusoidal Modulation Frequency = .133 and Damping Ratio = 1

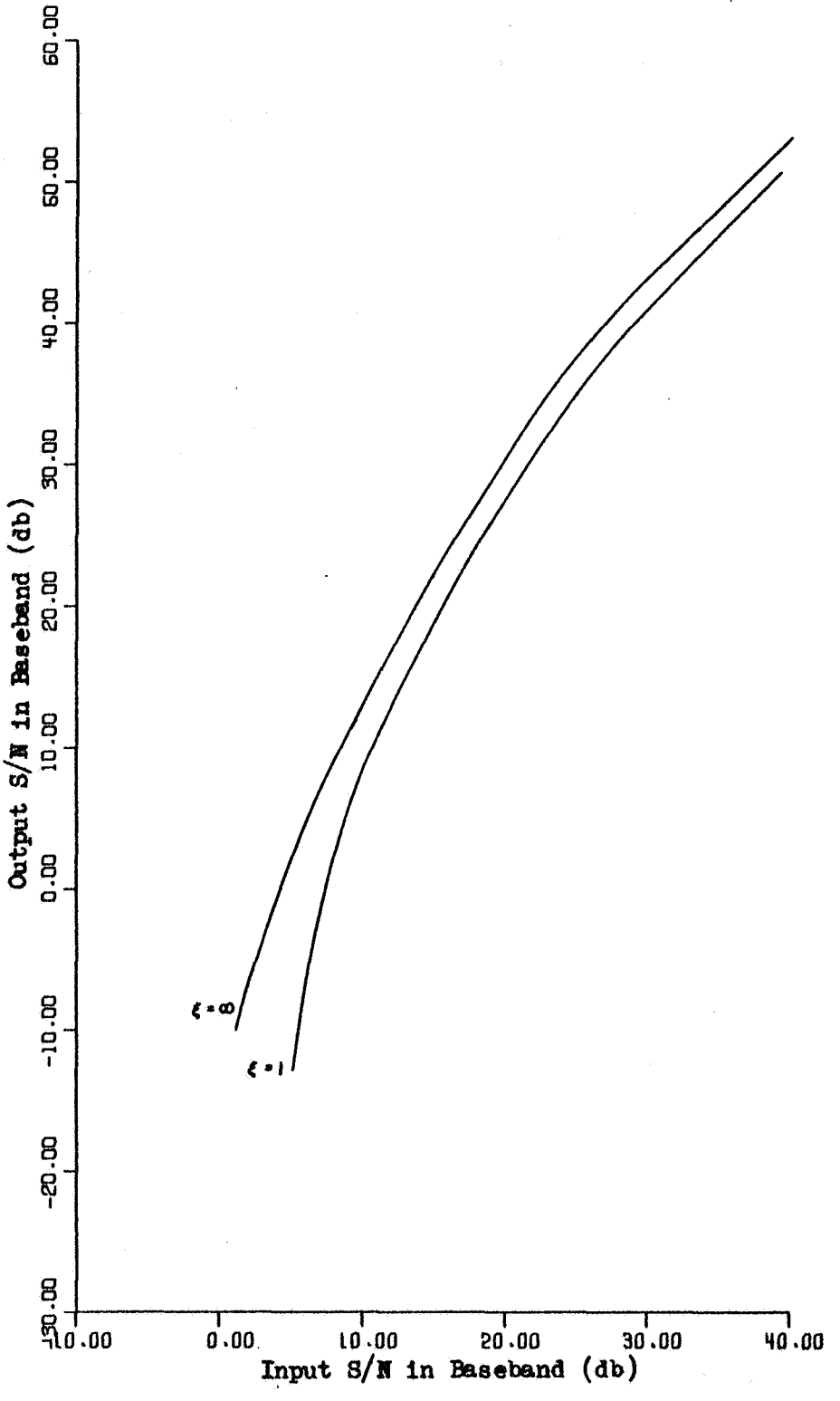

Figure 6.19. FM Threshold Curves for a Second Order PLL with Sinusoidal Phase Detector Characteristic and Several Damping Ratios

this section. Figure 6.20 is a block diagram of the test set up used to measure the I/O S/N data.

The random modulation originates in the GR 1390B noise generator. The modulation level or index is set by the left HP 350D attenuator. Because it is desirable to have the modulation spectrum flat down to zero frequency and since the GR 1390B has a low frequency cutoff of 5 Hz. it is necessary to frequency translate the noise generator spectrum. This is done by the Random Modulation Generator. Appendix F gives further details concerning the operation of this test fixture. The spectrum of the modulation is shaped by one section of the SKL 302 filter. This electronic filter has a controllable cutoff frequency and a 3 pole butterworth response. The noise generator also provides the random signal necessary for the channel noise. The spectrum of the noise is bandlimited and added to the modulated carrier as described in Section 6.2.1 and Appendix C. Since the spectrum of the noise used for the modulation and that used for channel noise do not overlap the two signals are independent. The output of the simulated IF drives the ELRPLL. The loop filter output of the ELRPLL drives the SKL 302 LPF. This filter has a 3 pole low pass butterworth linear response. Its 3 db cutoff frequency is adjusted to equal that of the modulation.

The modulation is also delayed by the two cascaded sections of the LH-42D for an amount of time equal to the delay of the combined channel and demodulator. It is important for this filter to not cause excessive frequency distortion of the modulation waveform. Since the delay per section of a low pass filter is inversely proportional to the cutoff frequency it's necessary to cascade the sections of the LH-42D in order to

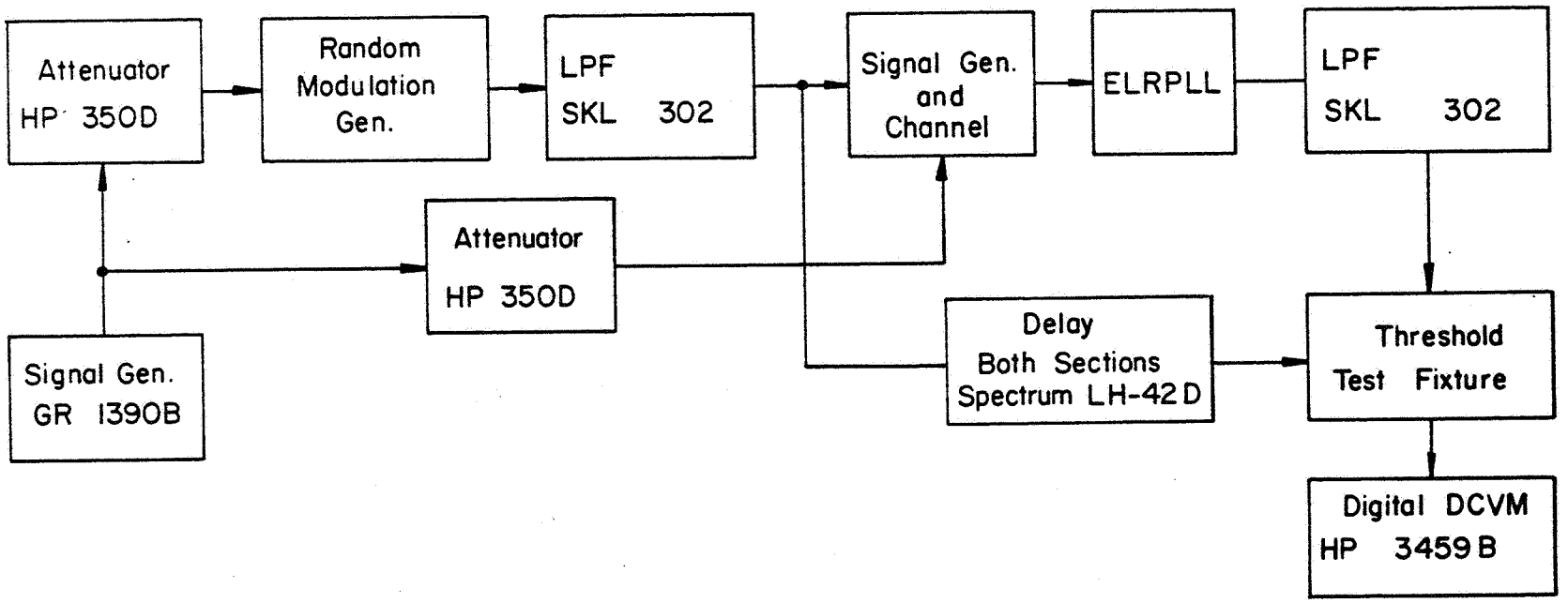

FIGURE 6.20. THRESHOLD TEST SET UP FOR RANDOM MODULATION.

have sufficient delay without frequency distortion. The same Threshold Test Fixture as used in Section 6.2.1 is used here to provide estimates of the signal and noise powers. These are measured by the digital DCVM as before. Appendix E describes this test fixture and the principles of its operation.

The data obtained in this manner is computer processed to correct for known measurement biases, such as meter loading of test circuits and non-ideally bandlimited channel noise spectrum. For further details see Appendix E. From the corrected data an estimate of the output S/N level in the output band is calculated. This data is plotted in Figures 6.21 through 6.26. In each figure the I/O S/N referred to the output band is plotted for several values of the modulation index. The same definitions used in Section 6.2.1 are used here.

Figures 6.21 through 6.23 are the I/O S/N curves of the second order ELRPLL for a modulation bandwidth of .133, damping ratio of 1 and N = 1, 2 and 8 respectively. The maximum output S/N level is limited by the frequency distortion caused by the ELRPLL transfer function.

Figures 6.24 through 6.26 are the I/O S/N curves of the second order ELRPLL for a modulation bandwidth of .067, damping ratio of 1 and N = 1, 2 and 8 respectively. The maximum output S/N level is also limited here by the frequency distortion caused by the ELRPLL transfer function but the limitation occurs at much higher index levels.

The threshold curves for the data in Figures 6.21 through 6.26 are plotted in Figure 6.27. The threshold at low input S/N is increased by decreasing N or decreasing B_m, the modulation bandwidth. For input S/N > 20 db the threshold is decreased by increasing N for the cases considered.

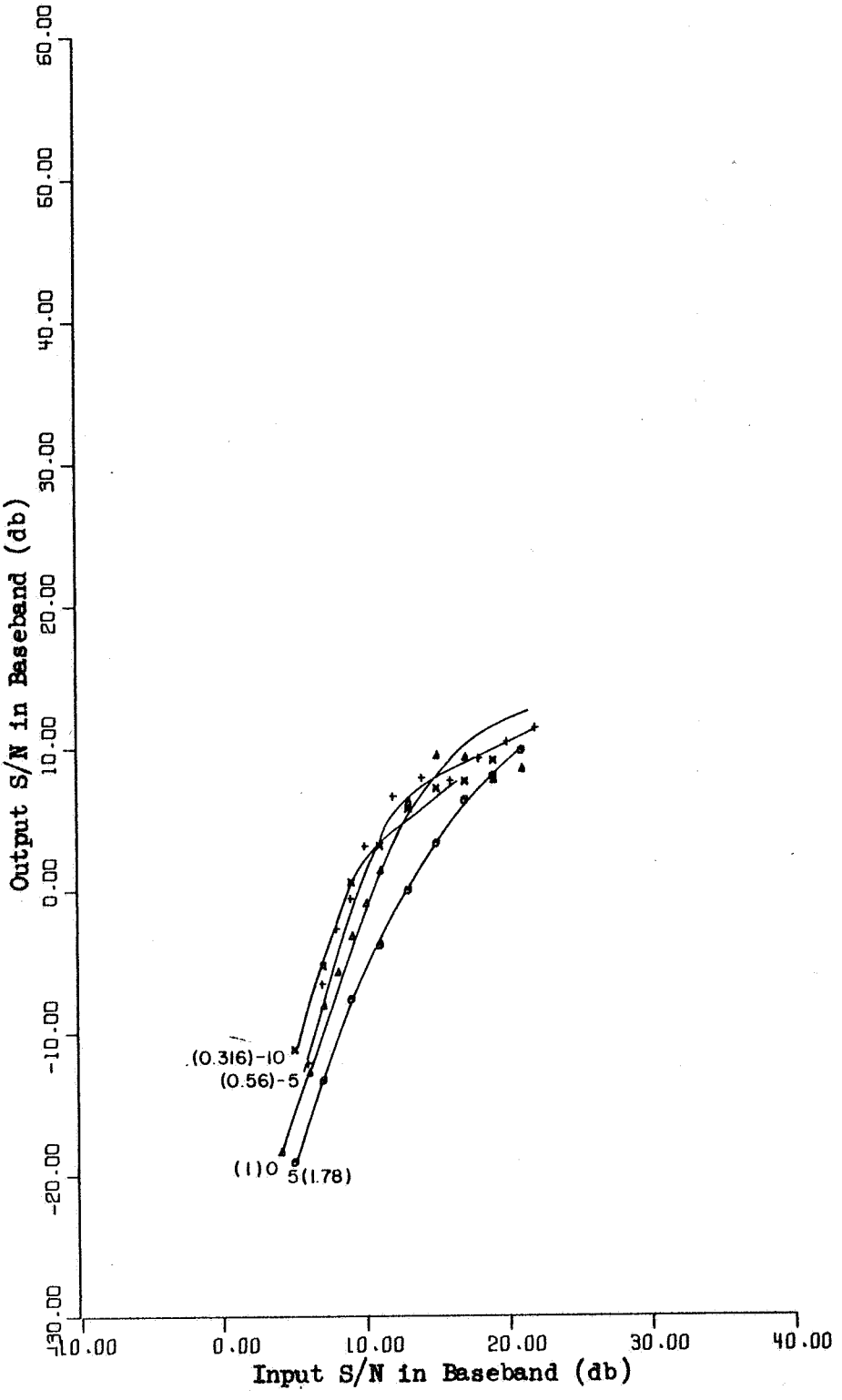

Figure 6.21. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .133 Bandwidth Random Modulation, Damping Ratio = 1 and N = 1

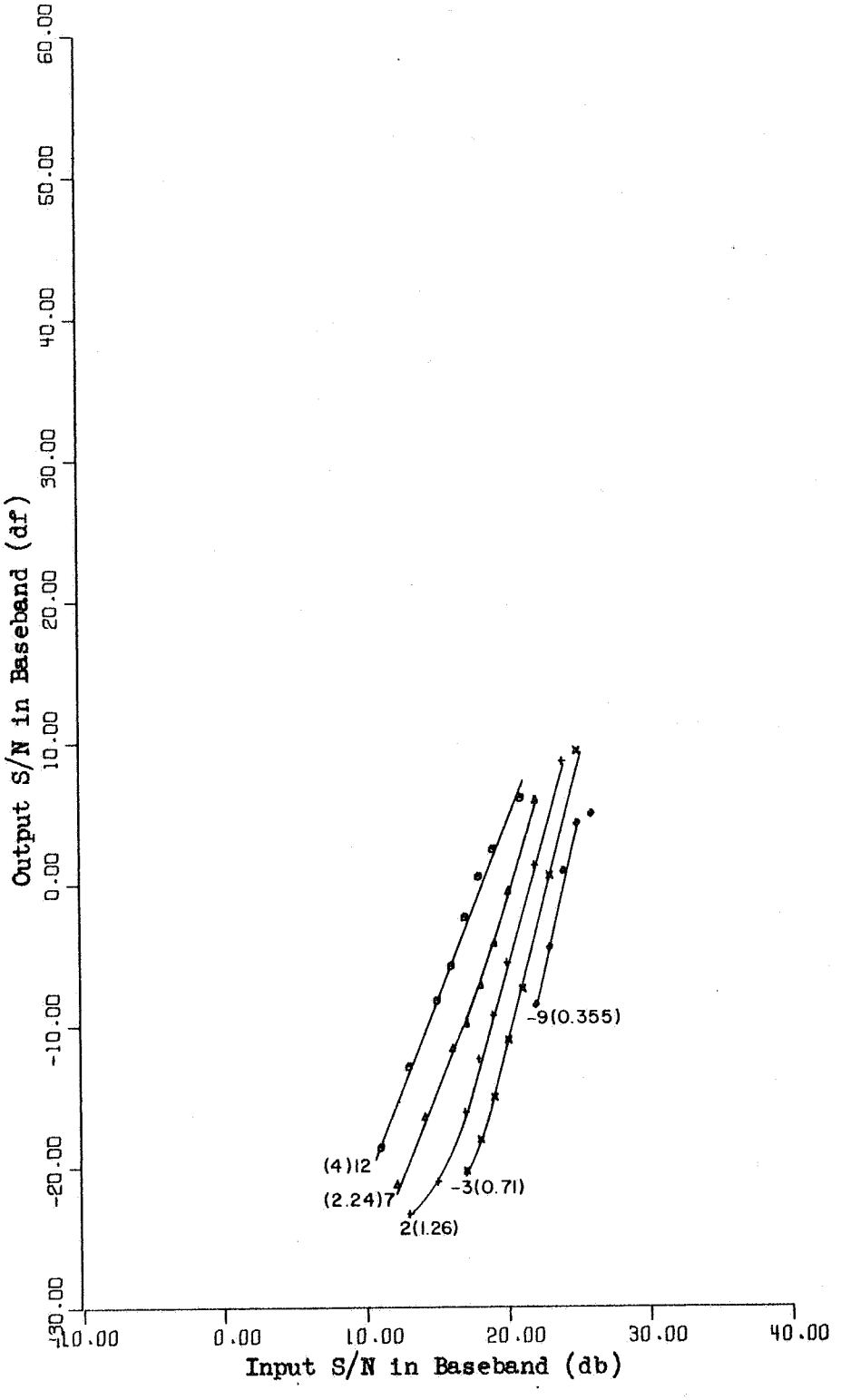

Figure 6.22. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .133 Bandwidth Random Modulation, Damping Ratio = 1 and N = 2

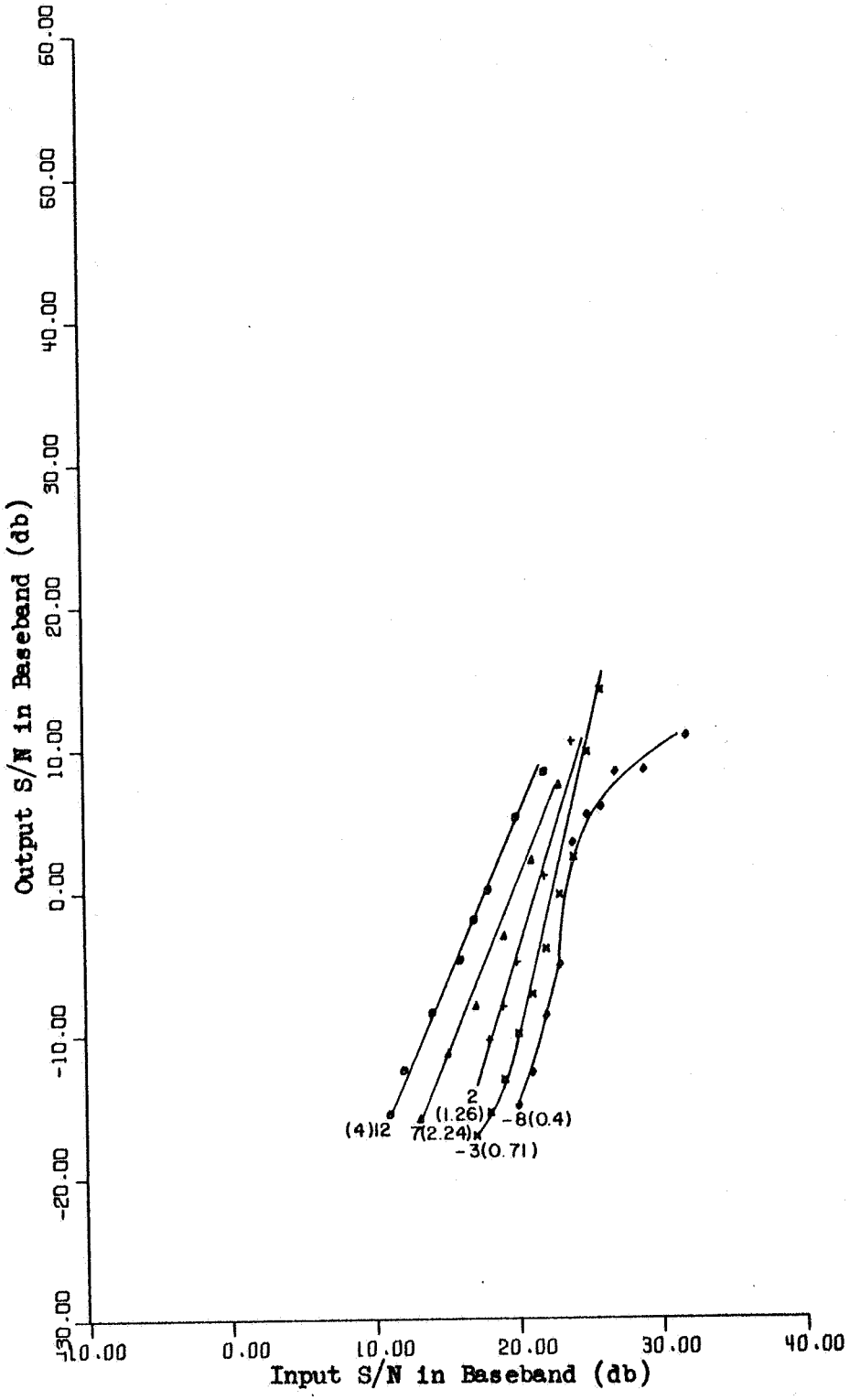

Figure 6.23. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .133 Bandwidth Random Modulation, Damping Ratio = 1 and N = 8

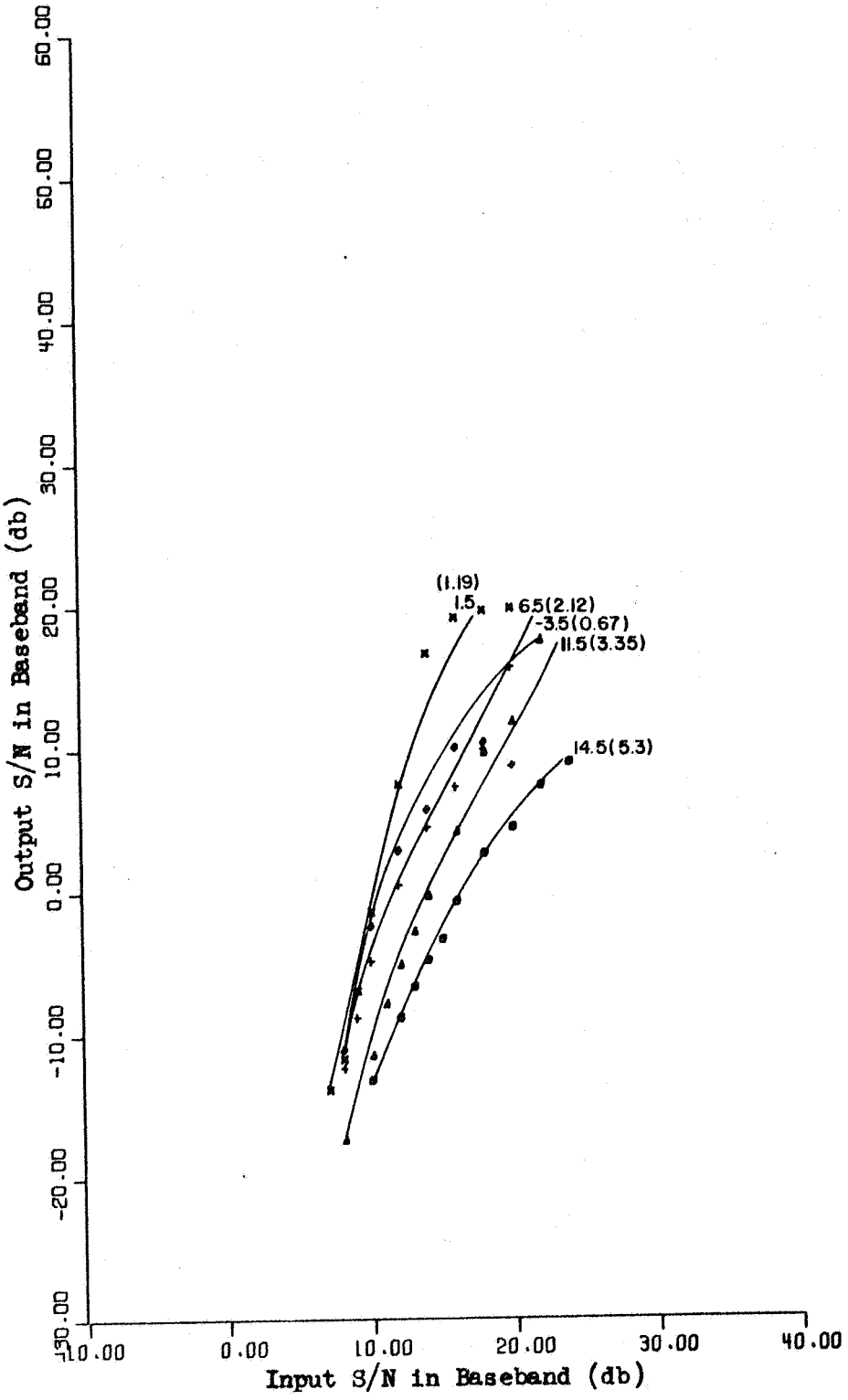

Figure 6.24. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .067 Bandwidth Random Modulation, Damping Ratio = 1 and N = 1

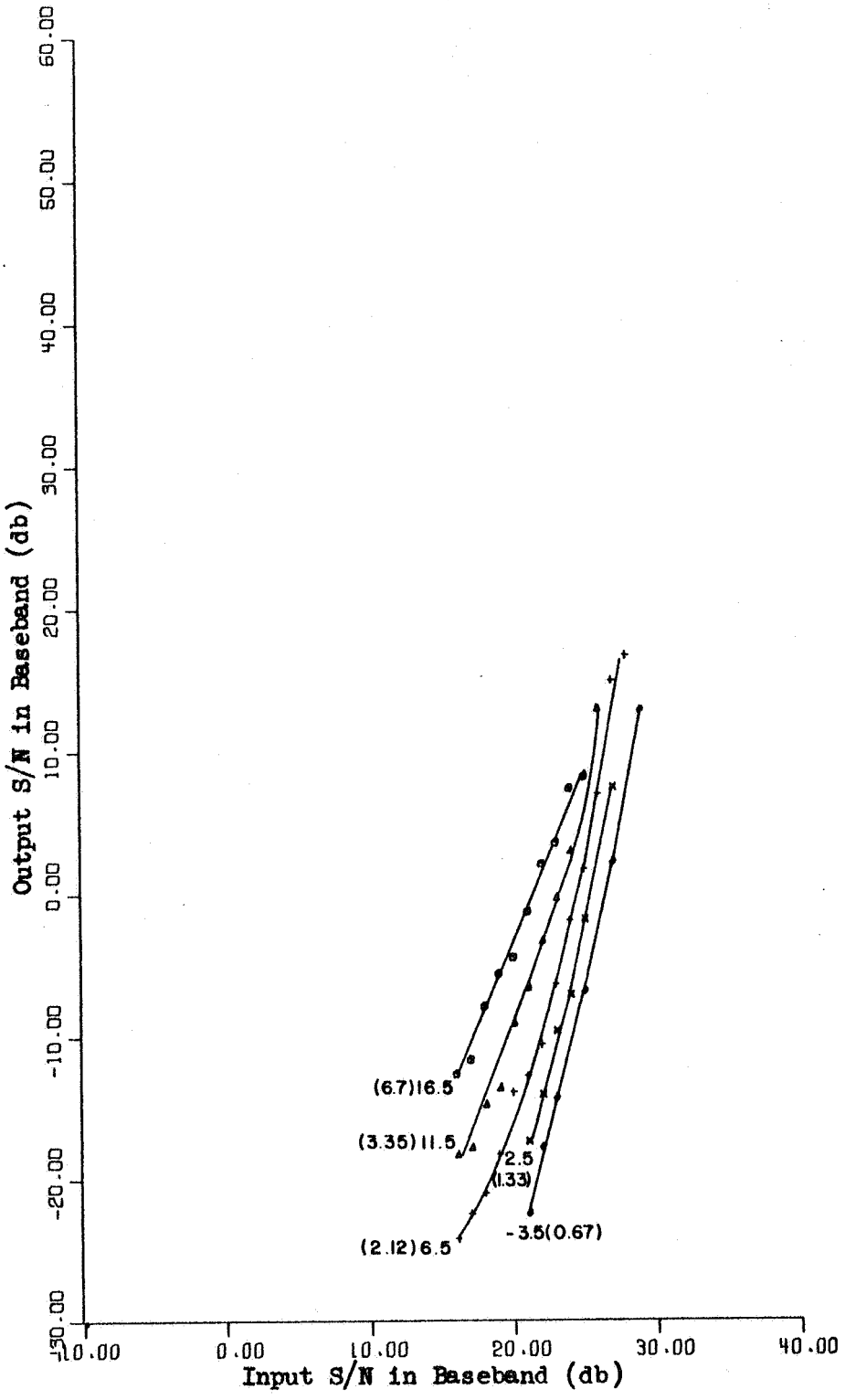

Figure 6.25. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .067 Bandwidth Random Modulation, Damping Ratio = 1 and N = 2

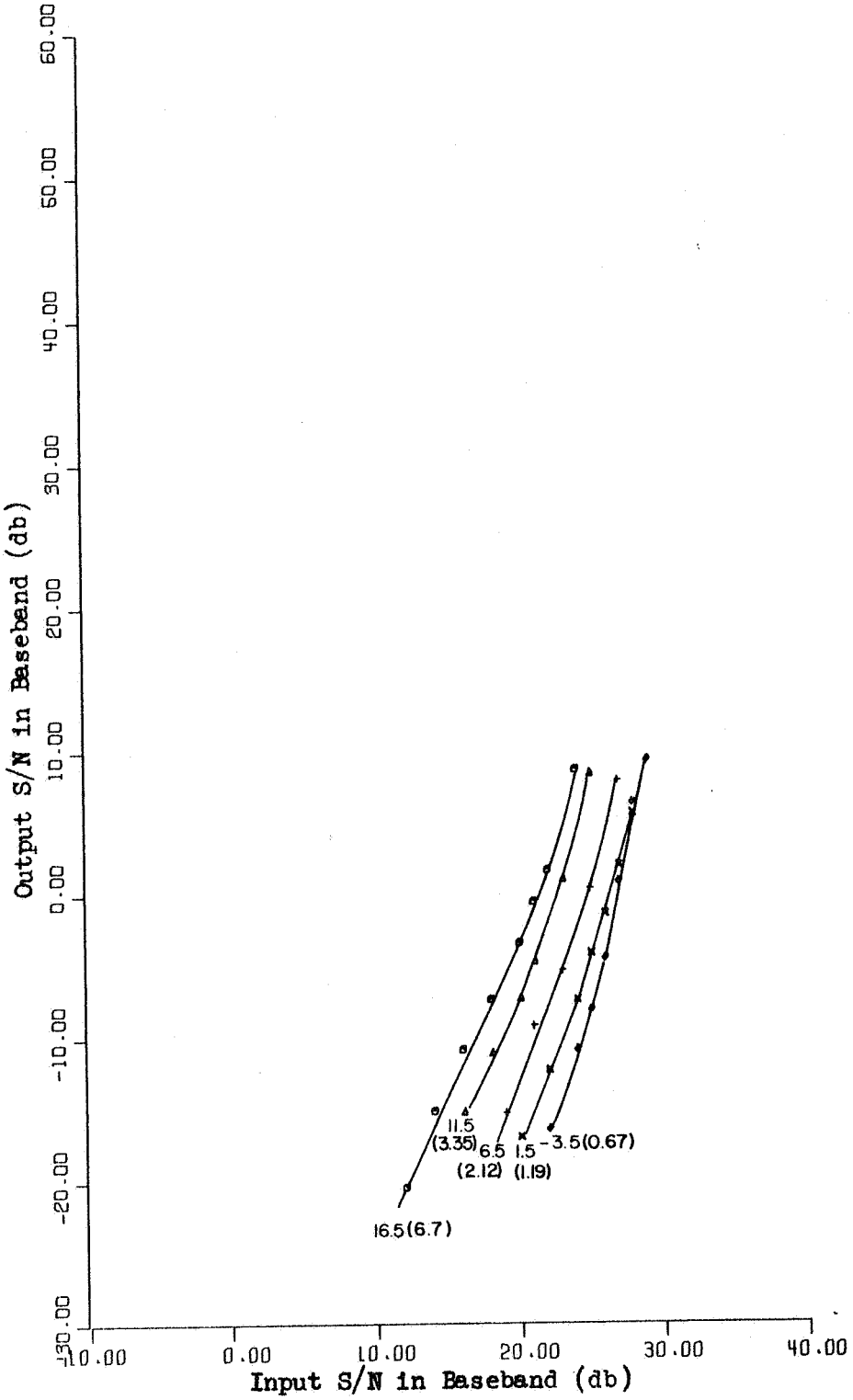

Figure 6.26. Input/Output S/N (Baseband) for a Second Order ELRPLL Using FM with .067 Bandwidth Random Modulation, Damping Ratio = 1 and N = 8

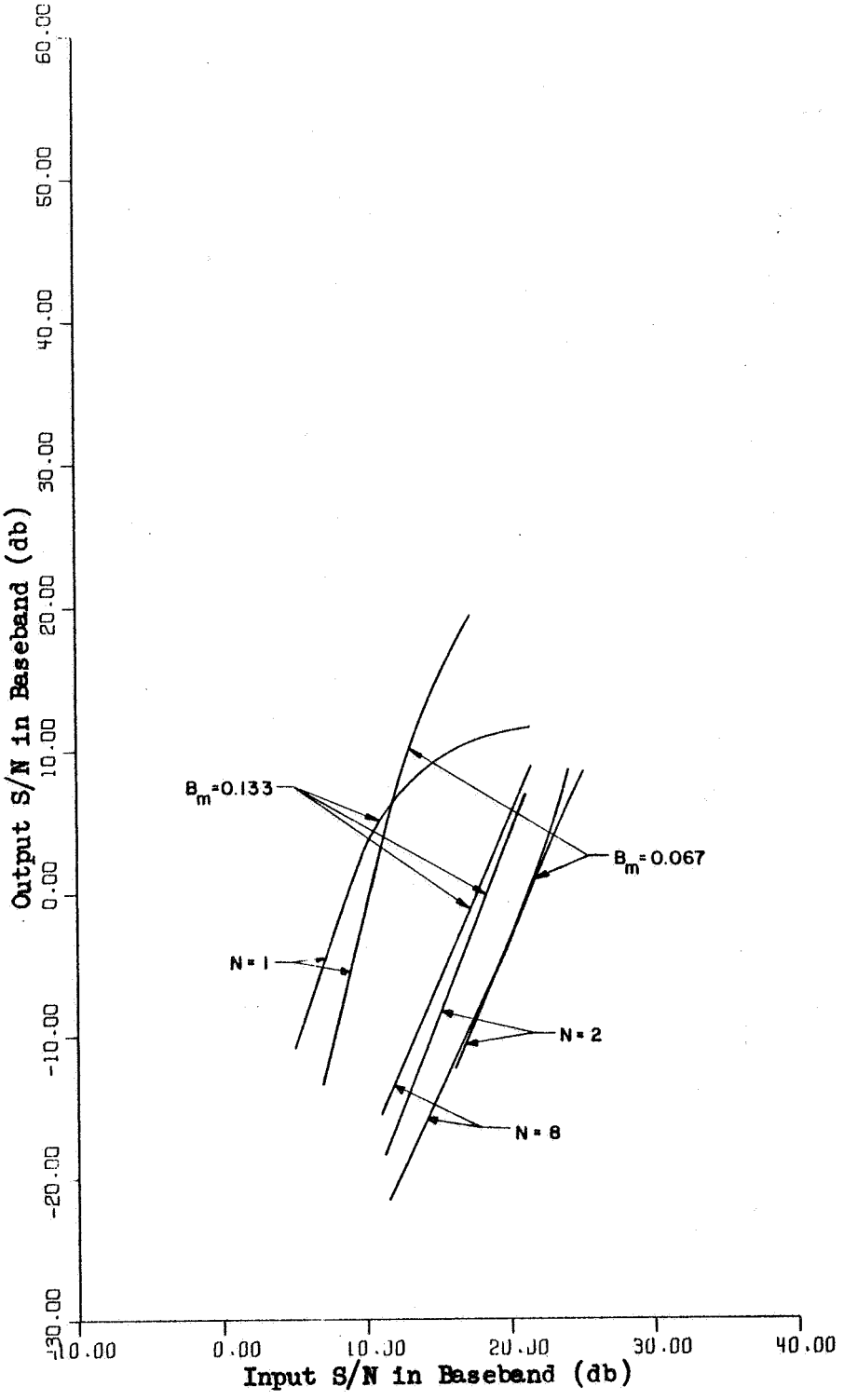

Figure 6.27. FM Threshold Curves for a Second Order ELRPLL with Damping Ratio = 1, Random Modulation and Several Values of N

Additional data is needed to determine absolutely whether the threshold curves for B_m = .067 cross. However one can infer from the cases in Figures 6.6, 6.16 and 6.27 for B_m = .133 that the threshold curves for B_m = .067 should cross but that this occurs at a higher output S/N level than for B_m = .133. It is estimated that the crossover takes place at an output S/N level of 23 db and an input S/N level of 26 db for B_m = .067. The crossover for B_m = .133 occurs at an I/O S/N of 23 and 13 db respectively. Therefore one can trade 3 db of low S/N threshold for a 10 db increase in output S/N level by increasing the loop bandwidth by a factor of 2.

Comparing Figures 6.6 and 6.27 it is readily apparent that the threshold of the ELRPLL is much higher for random modulation than for sinusoidal modulation. The threshold crossover point on the former is at 20 db input and 30 db output S/N levels. This is a 3 db threshold improvement with a 17 db output S/N level improvement. This means that the threshold of the ELRPLL is very sensitive to the type of modulation. The threshold of the ELRPLL for N = 1 is better than that of the PLL for sufficiently high input S/N levels and sinusoidal modulation. Since this improvement is caused by a reduction of the rate of cycle slips due to modulation, it is hypothesized that the ELRPLL has a lower threshold than the PLL for all types of modulation. However it is not clear how the ELRPLL compares with other types of demodulators such as FM feedback and the discriminator for the random and other modulation cases since the fundamental principles of operation of these devices are not generally comparable to those of the ELRPLL. Furthermore, this author has not found any investigation of their threshold properties for the random

modulation case. An important problem is that of signal modulation optimization for the particular demodulator being used. It appears that one can gain several db of threshold improvement just by choosing the right form of modulation.

Several attempts were made to determine a theoretical model for the FM threshold of the ELRPLL. The traditional approaches such as Boontoon's technique [2] and the quasi-linearization approaches [11, 30] require a priori knowledge of phase error PDF. The ELRPLL contains a non-linearity as well as feedback which modify the PDF of the signal from point to point within the loop. In view of this, these techniques were not used.

Finally an attempt was made to determine the rate of $2N\pi$ cycle slips. It is felt that a first order approximation to the output noise power can be made if the power that the noise due to $2N\pi$ cycle slips adds to the ELRPLL output is known. However this analysis has not yet proved to be mathematically tractable. This technique is discussed further in Chapter VII.

VII. CONCLUSIONS

This chapter discusses and compares the results obtained in Chapters III, V and VI. It also contains a discussion of problems for further study. The chief problem for further study is the theoretical FM threshold of the general PLL. A brief outline is made of a technique that may lead to a solution of the theoretical threshold for a large class of first order PLL.

Section 7.1 discusses, compares and presents conclusions concerning the ELRPLL acquisition time. Section 7.2 deals similarly with the experimental results for the FM threshold. Section 7.3 outlines areas for further study of the ELRPLL and of the PLL in general.

7.1. Acquisition Time

The data obtained in Chapters III and V is compared in this section. The theoretical acquisition time data in Figure 3.9 for the case of zero initial phase error is compared with the normalized high S/N experimental data obtained in Section 5.2 and the high S/N regression analysis model, equation (5.7), in Figures 7.1, 7.2 and 7.3 for the case of ξ = .5, 1 and 2 respectively. In each case the straighter of the two lines is the theoretical result.

The theoretical and experimental results agree very closely except when $|\Delta f'|/N$ is large. The experimental system long term stability was not sufficiently good to obtain accurate acquisition time data for cases

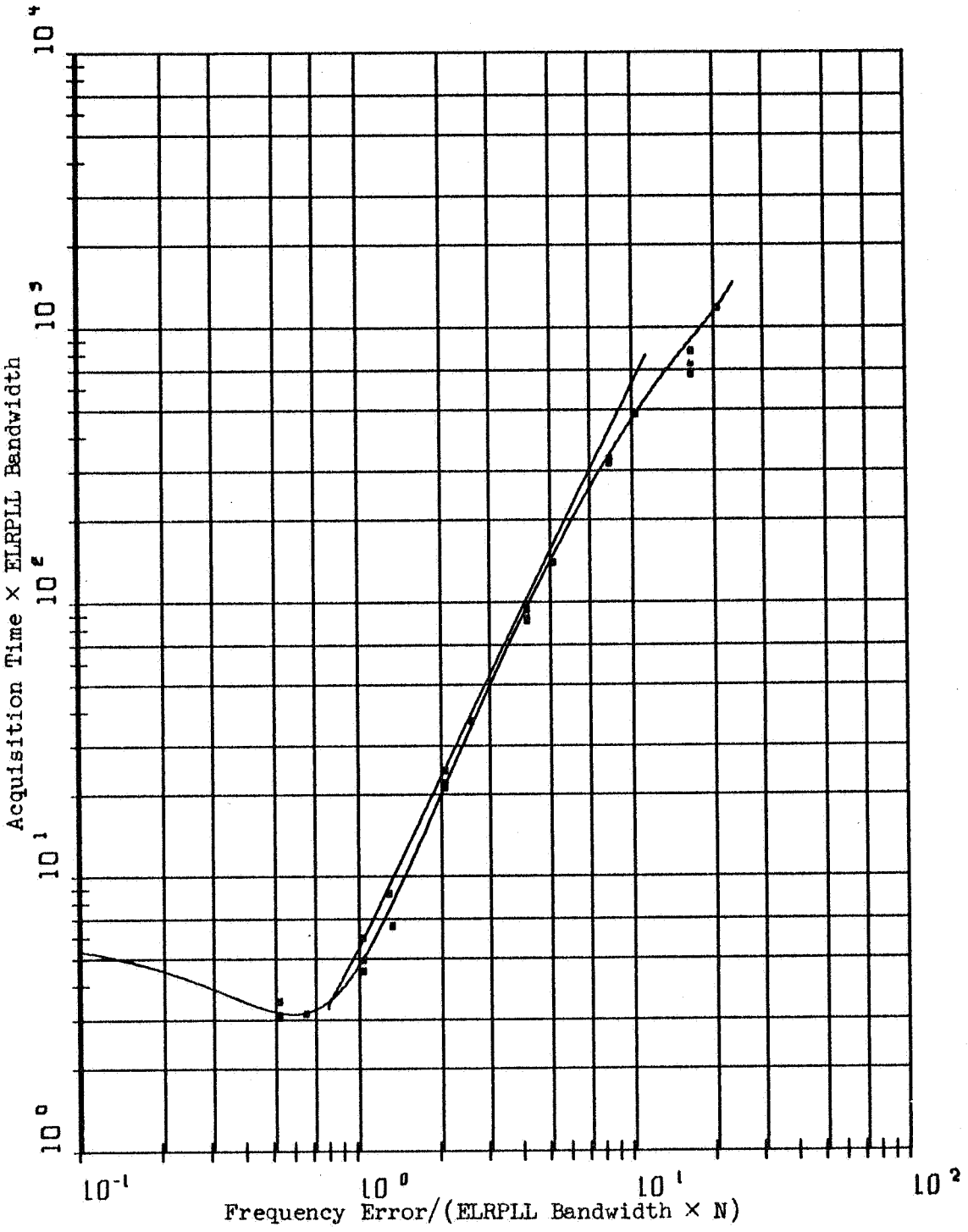

Figure 7.1. Comparison of a Second Order ELRPLL Experimental and Theoretical Acquisition Time versus the Initial Frequency Error for High S/N and a Damping Ratio = .5

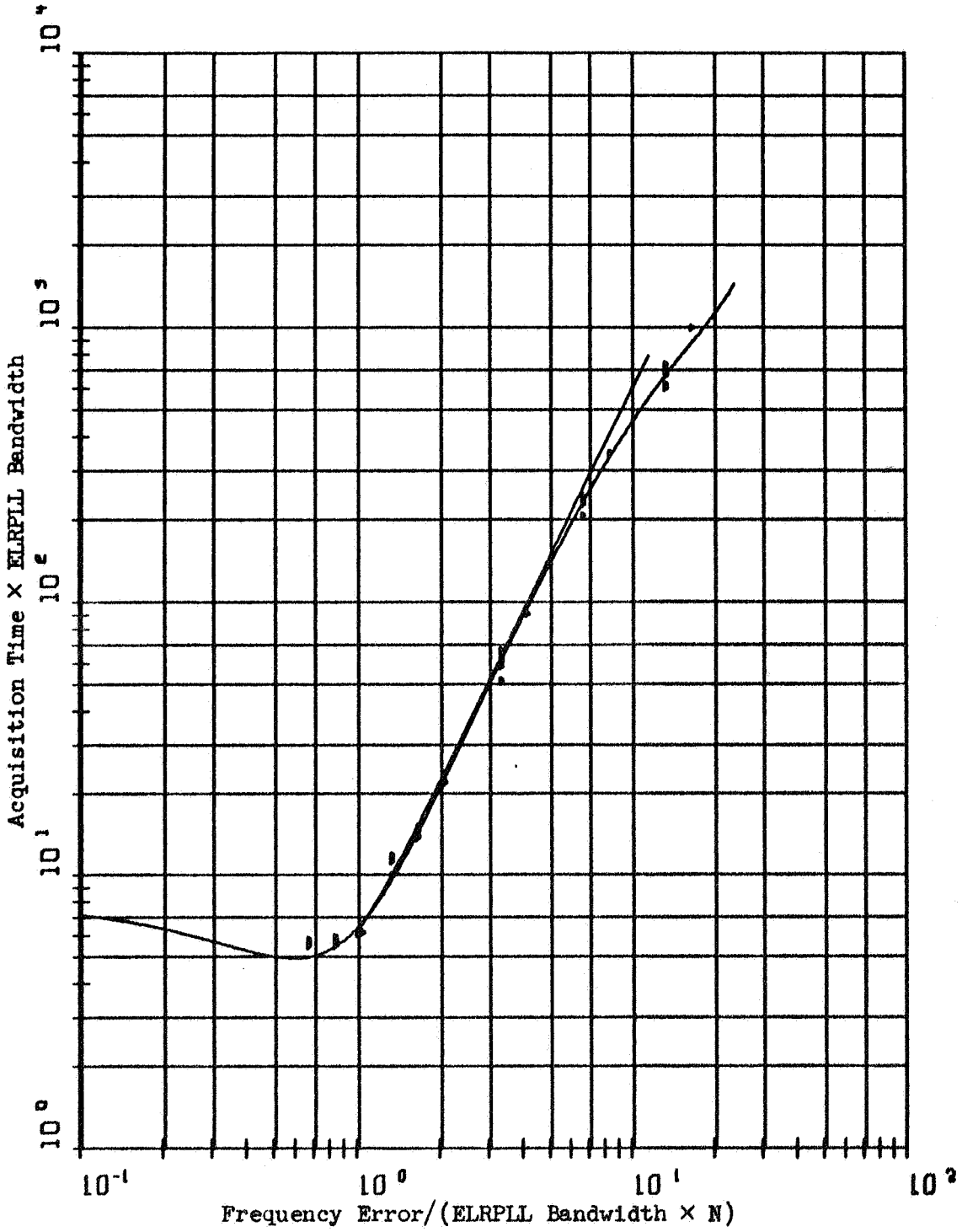

Figure 7.2. Comparison of a Second Order ELRPLL Experimental and Theoretical Acquisition Time versus the Initial Frequency Error for High S/N and a Damping Ratio = 1

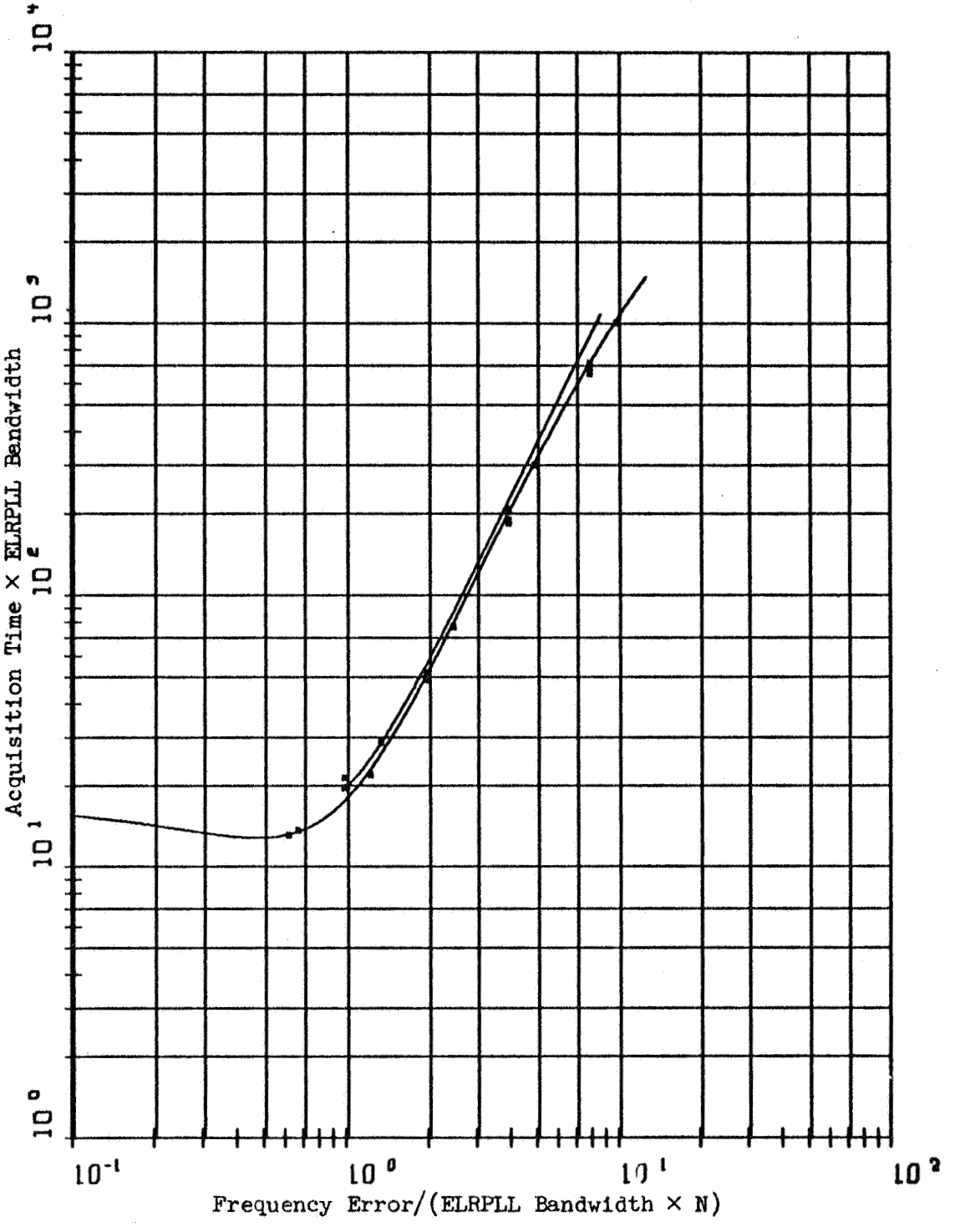

Figure 7.3. Comparison of a Second Order ELRPLL Experimental and Theoretical Acquisition Time Versus the Initial Frequency Error for High S/N and a Damping Ratio = 2

when the time was greater than 10 seconds. It was noticed that for the case of no channel noise the variance of the acquisition time for data greater than 10 seconds was as much as 100 times larger than that for shorter times. Theoretically the variance should be zero for the no noise case. The variation was due to the experimental system drift. Had these problems not existed it is believed that the acquisition time data would asymptotically approach a quadratic dependence upon $|\Delta f'|/N$ for large $|\Delta f'|/N$ and the high S/N case. The theoretical ELRPLL high S/N acquisition time asymptotes have a slope of 2 on the log-log plots. Therefore the asymptotic dependence upon $|\Delta f'|/N$ is quadratic and the improvement in acquisition time is

$$T_a = T_s K_1/N^2 = .149\ T_s/N^2 \ . \tag{7.1}$$

In Section 3.6 and Table 3.1 the large $|\Delta f'|/N$ and high S/N acquisition time dependence on ξ is the same as that for a PLL. Therefore

$$T_a \simeq .149\pi^2(1 + 4\xi^2)^3\Delta f^2/32\xi^4N^2B_L^3 \ , \tag{7.2}$$

for $|\Delta f|/NB_L > 1$ and input S/N $\gg$ 0 db. The acquisition time improvement of the ELRPLL over a PLL is very significant even for the case of N = 1.

There is no theoretical low S/N acquisition time analysis. The experimental acquisition time regression analysis gives a model that estimates the average acquisition time of the ELRPLL for S/N > 0 db. However the dependence upon $\Delta f'$, N and f_c'' is not accurate for large N and f_c''. For the data obtained, an upper bound on the average acquisition time is given from (5.11),

$$\hat{T}_a \leq \hat{T}_{ah}\ \mathrm{Exp}[1800\ N/S] \tag{7.3}$$

For most cases (7.3) is an extremely conservative bound. There are

a few cases for which the acquisition time is a decreasing function of N/S. This occurs for some situations when the cycle slips due to noise and those due to frequency error are in the opposite direction or in other words if

$$f_v > f_c > f_0 \text{ or } f_0 > f_c > f_v \tag{7.4}$$

The data in Figures 5.3 through 5.9 indicates that the acquisition time for a given input S/N level is lowest for $f_c'' = 0$. Therefore it is desirable to have the carrier frequency near the center of the input band. It appears that the greater that $|f_c''|$ is, the greater the effect of input noise upon acquisition time. The effect of N, ξ, B_L, Δf and f_c'' upon T_a is very complex and that of each of these parameters is not independent of the other.

When 7.4 is not true, there is an input S/N level below which acquisition does not always occur. This was experimentally observed when the loop would only acquire synchronization on some of the trials for these parameter values. The probability of synchronization appears to be a rapidly decreasing function of N/S for these cases when N/S exceeds a critical level.

7.2. FM Threshold

The threshold curves presented in Chapter VI are summarized and conclusions concerning the threshold phenomenon are made in this section. First the sinusoidal modulation threshold is considered and then that for white, bandlimited, gaussian, random modulation.

From Figure 6.6 it is concluded that the ELRPLL has a lower threshold than the PLL for sinusoidal modulation frequency of .133 and loop

damping ratio = 1 when the input S/N level is greater than 14 db. When the input S/N level is greater than 20 db the threshold is improved by making N greater than 8. The data indicates that the low S/N threshold can be exchanged for the high S/N threshold by increasing N. It appears that one can improve threshold for a given level of S/N input by choosing an optimum value of N.

From Figure 6.9 it is concluded that for $\xi \leq 1$ the threshold is a decreasing function of ξ for $f_m = .133$ and N = 1. However for $\xi > 1$ there is little change in the threshold for input S/N levels between 13 and 25 db. Above 25 db it is possible to reduce the threshold by increasing ξ without limit. The limiting case of $\xi = \infty$ corresponds to the first order loop.

From Figure 6.13 it is apparent that the low input S/N threshold can be traded for high input S/N threshold by increasing the loop bandwidth B_L. A 2 to 1 increase in B_L produces about the same decrease in high input S/N threshold as a 2 to 1 increase in N. The critical level of input S/N is about 17 db. Above this level, increasing B_L is effective in reducing threshold.

Figure 6.16 shows the effect of N upon the threshold of the first order ELRPLL with sinusoidal modulation of .133 frequency. When the input S/N is greater than 22 db increasing N will reduce the threshold. The effect here is similar to that for the second order loop. Again the threshold of the PLL is at best only 2 db better than the ELRPLL and for input S/N greater than 22 db the ELRPLL has a lower threshold than the PLL.

The threshold of the PLL with a sinusoidal phase detector

characteristic is given in Figure 6.19. The first order loop exhibits a 2 db threshold advantage over the second order loop for $\xi = 1$, and sinusoidal .133 frequency modulation.

The random modulation case in Figure 6.27 has a threshold crossover point at 23 db input S/N for $B_m = .133$ and probably near 26 db for $B_m = .067$. When the input S/N level is greater than 12 db and N = 1, the threshold of the ELRPLL for $B_m = .067$ is lower than that for $B_m = .133$. In general one can optimize B_m or N for lowest threshold just as can be done with sinusoidal modulation. However the optimum values are not necessarily the same.

In general the following statements can be made for the ELRPLL threshold with sinusoidal or random modulated signals. The threshold can be changed by two mechanisms. By increasing B_L or N or both one can trade low input S/N threshold for high input S/N threshold. There exists an optimum value of either parameter, in terms of lowest threshold, for each input S/N level. Either parameter can be used to optimize threshold but from the practical standpoint of system simplicity it is easier to use B_L. This is exactly what Jaffe and Rechtin [11] propose for optimizing the standard PLL. From the standpoint of frequency and intermodulation distortion of the output of the ELRPLL, it is advantageous to use the largest value of B_L consistent with other requirements. Further it is concluded that for input S/N greater than 14 db it is better to use the ELRPLL than the PLL since the former has a lower threshold even for N = 1.

Similarly, the acquisition time of the ELRPLL can be changed by two mechanisms. By increasing B_L or N or both one can reduce the acquisition

time. However, here there is a theoretical reason for choosing B_L in preference to N. B_L has an inverse cubic effect upon the acquisition time but N only has an inverse quadratic effect. The ELRPLL for N = 1 has a high S/N acquisition time that is .149 times as long as that for the PLL. This author could not find any study of the low S/N acquisition time of a PLL with a constant plus integral filter. Therefore, a comparison is not made for the low S/N ELRPLL acquisition time case.

Based on these conclusions it appears that the ELRPLL has a significant threshold, acquisition time, and intermodulation distortion advantage over the PLL. The last of these advantages was not investigated here but it is rather clear that a more linear system will cause less distortion than a less linear one.

7.3. Areas for Further Study

This section poses several questions that need further investigation concerning both the general PLL and the ELRPLL.

7.3.1. Low S/N Acquisition Time

Further work is necessary on the experimental acquisition time. Additional data is needed to improve the regression analysis model. In particular the effects of Δf and f_c'' need further consideration.

At the time of this writing there is no theoretical low S/N acquisition time model. This appears to be a very difficult problem because of the complications caused by the random cycle slip phenomenon.

7.3.2. Threshold

An attempt was made in this study to obtain a theoretical threshold result for the ELRPLL. The approach is to determine the noise in the

output band of the ELRPLL due to cycle slips of $2N\pi$ radians. It is hypothesized that threshold begins to occur when this portion of the output noise power is of the same order of magnitude as the gaussian component predicted by linear analysis.

In order to determine this noise power the rate of $2N\pi$ radian cycle slips must be determined. The phase error space is divided into M adjacent equal length intervals. The transition probabilities of ϕ_e jumping between the ith and jth regions in Δ time are calculated. Assuming that ϕ_e is a stationary random walk, the process of jumping between regions is a stationary Markov chain. From these probabilities the solution of an Mth order matrix equation yields the probability mass function of ϕ_e being within each region. The rate of $2N\pi$ radian cycle slips can be calculated from the probability mass function and the transition probabilities.

The difficult problem here is the calculation of the transition probabilities. This involves the integration of a four dimensional gaussian probability density function. The following development gives the integral.

The probability of ϕ_e jumping from the ith to the jth region in Δ seconds is

$$P_{j/i} = P_{ij}/P_i \ , \tag{7.5}$$

where P_{ij} is the joint probability of being in the ith region at t and in the jth region at $t + \Delta$ for all t and P_i is the probability of being in the ith region.

Then P_{ij} is given by

$$P_{ij} = P[\phi_e(t + \Delta) \subset \phi_i, \ \phi_e(t) \subset \phi_j] \ , \tag{7.6}$$

where

$$\Phi_i = \{i < M\Phi_e/2N\pi \leq i + 1\}. \tag{7.7}$$

The joint density function of $[\Phi_e(t), \Phi_e(t + \Delta)]$ is more easily handled in the rectangular coordinates of the multiplier output variables of Figure 4.1 since they are jointly gaussian when the loop is open. After a rotation of this coordinate system by angles of $2iN\pi/M$ and $2jN\pi/M$ radians the joint probability is

$$P_{ij} = \int_0^\infty dx_1 \int_0^\infty dx_2 \int_0^{\alpha x_1} dy_1 \int_0^{\alpha x_2} dy_2 \, f_{ij}(x_1, x_2, y_1, y_2), \tag{7.8}$$

where $\alpha = \mathrm{Tan}(2N\pi/M)$, the subscript "1" refers to variables at t and "2" refers to variables at $t + \Delta$. $f_{ij}(x_1, x_2, y_1, y_2)$ is the joint density of the multiplier outputs at the two times corresponding to the (i,j) rotation. However the evaluation of this integral does not appear to be mathematically tractable at this time. It may be solvable using numerical integration and this should be investigated.

If this integral can be evaluated, it may be possible to determine the joint density of $[\Phi_e(t), \Phi_e(t + \Delta)]$ and hence calculate the total output power of an ELRPLL demodulator for the first order case. It may also be possible to consider a larger class of phase detector characteristics.

All the experimental threshold work in this study is for the case when the carrier is centered in the input noise spectrum. It is intuitively felt that this yields the best threshold. It would be useful to determine the threshold when the carrier is not centered.

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APPENDICES

APPENDIX A

THEORETICAL ACQUISITION TIME COMPUTER PROGRAM

Appendix A contains a description of the computer program used to obtain the ELRPLL high S/N transient response and acquisition time for a frequency step of the input signal.

In the text the differential equation describing the normalized ELRPLL and the three cases of solutions are developed. Starting at this point, in order to calculate the transient phase error, it is necessary to solve a set of non-linear equations for the times that certain boundary conditions are met. These boundary conditions are

$$\dot{\phi}_e'(\tau_i^+) = \dot{\phi}_e'(\tau_i^-) + \phi_e'(\tau_i^-)\,\frac{2\xi}{a} \qquad (A.1)$$

and

$$\phi_B'(\tau_i^+) = \phi_B'(\tau_i^-),\ i = 1, \cdots, K. \qquad (A.2)$$

To make the program efficient in terms of computer time the following procedure is used. Figure A.1 is an abbreviated flow chart of this procedure. The number of cycles that the ELRPLL slips during acquisition is related to the initial frequency error. However in general the range of frequency error that can occur at the time of the last cycle slip is finite and does not depend upon the initial frequency error or phase error but only upon the loop damping ratio.

This can be shown by the following argument. Without loss of generality, it is sufficient to only consider the case of positive frequency

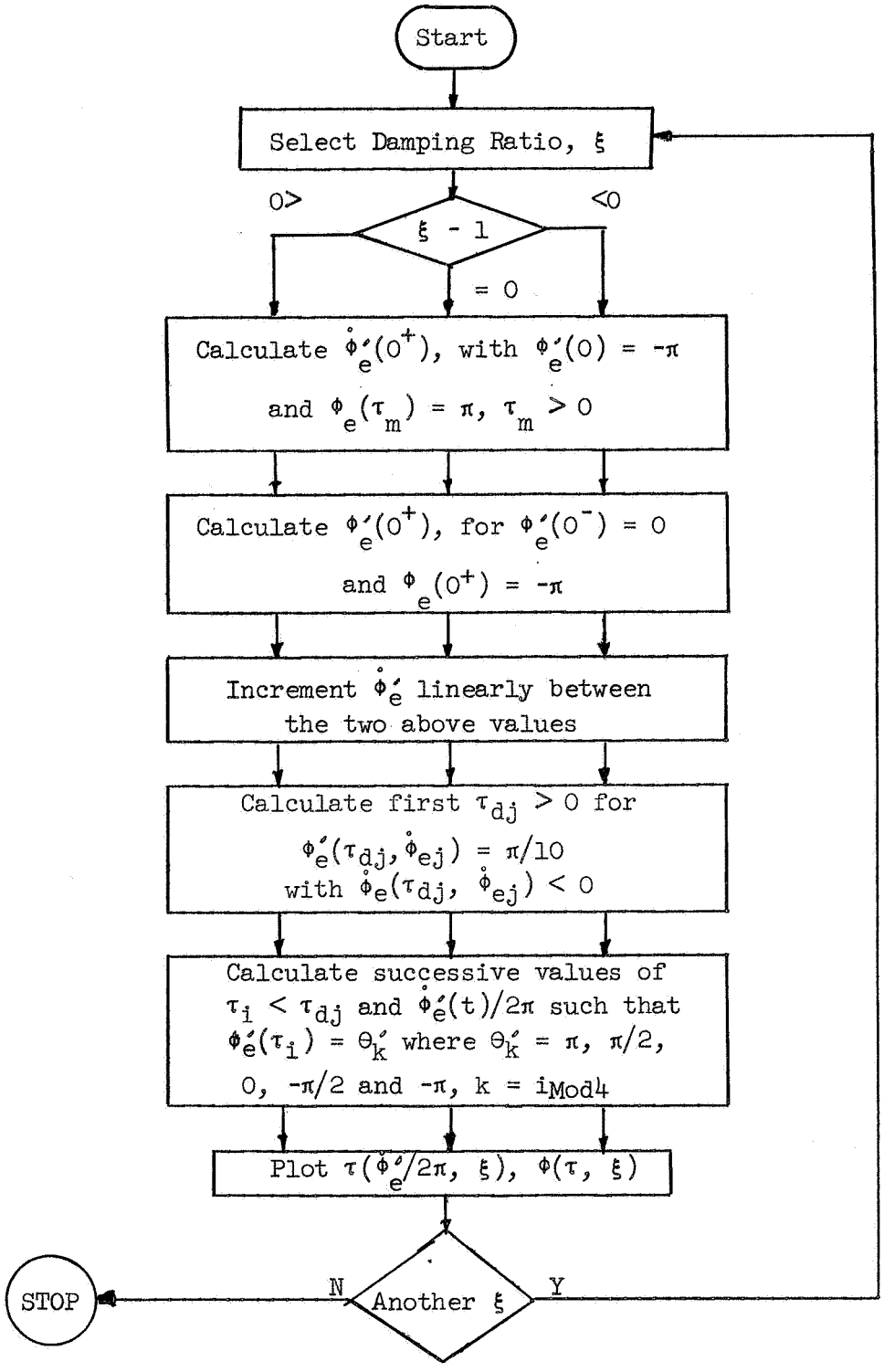


Figure A.1. Theoretical Acquisition Time Computer Program Flow Chart

error because of the phase detector's odd symmetry. If the frequency error is sufficiently great at the start of the ith cycle slip it will be greater than zero at the beginning of the i + 1st cycle slip. If it is greater than zero when the phase error is in some arbitrarily small neighborhood of π, then a cycle slip will occur. However if the frequency error is less than a certain critical value at the ith cycle slip then the frequency error will pass through zero when the phase error is less than π and no further cycle slips will occur. The maximum frequency error at the end of the last cycle slip is found by first solving the following set of equations:

$$\phi'_e(0^+) = -\pi \,, \tag{A.3}$$

$$\phi'_e(\tau_m) = \pi \,, \tag{A.4}$$

$$\dot{\phi}'_e(\tau_m) = 0 \,. \tag{A.5}$$

These are solved using Newton's Iteration for A, B and τ_m, where τ_m is the smallest $\tau > 0$ satisfying (A.3) through (A.5). Then the maximum phase error at the end of the last cycle slip, $\phi'_e(0^+)_{max}$, is found by determining $\phi'_e(0^+)$ for the A and B obtained from (A.3) through (A.5). The minimum frequency error at the beginning of the last cycle slip is essentially zero. Therefore by (A.1)

$$\dot{\phi}'_e(0^+)_{min} = 2\pi\xi/a. \tag{A.6}$$

A set of $\dot{\phi}'_{ej}(0^+)$, $j = 1, \cdots, 5$, where

$$\dot{\phi}'_{ej} = \dot{\phi}'_e(0^+)_{min} + \frac{\dot{\phi}'_e(0^+)_{max} - \dot{\phi}'_e(0^+)_{min}}{4}(j - 1) \,, \tag{A.7}$$

is calculated. Then the decay time τ_{dj}, $j = 1, \cdots, 5$ is calculated for

each $\dot{\phi}_{ej}$ where τ_{dj} is the first τ for which

$$\phi'_e(\tau) = \pi/10 \qquad (A.8)$$

and

$$\dot{\phi}'_e(\tau) < 0 \qquad (A.9)$$

subject to the initial conditions

$$\phi'_e(0^+) = -\pi \qquad (A.10)$$

and

$$\dot{\phi}'_e(0^+) = \dot{\phi}'_{ej} \quad . \qquad (A.11)$$

Then stepping backwards in time the program computes using Newton's Iteration the times at which ϕ'_e is $\pi/2$, 0, $-\pi/2$, and $-\pi$ radians in succession. It also calculates the frequency error, Δf, at each of these points. At the point $\phi'_e = -\pi$ the phase boundary is reached and the boundary conditions are imposed to obtain $\dot{\phi}'_e$ and ϕ'_e for the time just after this point where $\phi'_e = \pi$. This process is repeated for 6250 cycle slips by the program. The set of τ, $\dot{\phi}'_e$ and ϕ'_e obtained can be used either to plot the acquisition time curves, $\Delta f(T_a = \tau_{dj} - \tau)$, or the transient response, $\phi'_e(\tau_K - \tau)$. τ_K is the time of the cycle slip corresponding to the desired initial $|\Delta f'|$.

These two procedures are used to obtain Calcomp plots of the acquisition time and phase error transient response. The former is used for values ξ = .25, .35, .5, .71, 1.0, 1.41 and 2 and for values of $\phi'_e(0) = -\pi, -\pi/2, 0, \pi/2, \pi$, and the latter for the case of $\phi'_e(0) = 0$, and ξ = .35, .5, .71, 1.0, 1.41, and $\Delta f(0) = 2$.

APPENDIX B

EXPERIMENTAL ELRPLL SYSTEM

Appendix B describes the technical details and alignment procedures for the experimental ELRPLL system. Each circuit diagram and its alignment procedure is presented and discussed.

B.1. The VCO

Figure B.1 is the circuit diagram of the VCO. The VCO specifications are: 1. the short term frequency instability is less than 1 Hz./sec. and the long term frequency instability is less than 30 Hz./day; 2. the frequency range is 95 to 105 KHz.; 3. the voltage to frequency conversion linearity is better than 1%; 4. the VCO has less than 1 Hz. residual FM above 1 Hz. bandwidth; 5. the frequency dependence upon the supply voltage is less than 10 Hz./V; 6. the two quadrature outputs are within .01 radians of being in perfect phase quadrature over the VCO frequency range; 7. the logic levels of the two outputs are greater than three volts for the one's case and less than .5 volts for the zero's case.

In order to provide adequate power supply isolation a two stage positive voltage regulator and a one stage negative voltage regulator are used. The first stage of the former and the latter regulators are located in the upper left corner of Figure B.1. Each regulator is a standard negative feedback type. An error voltage, generated by zener

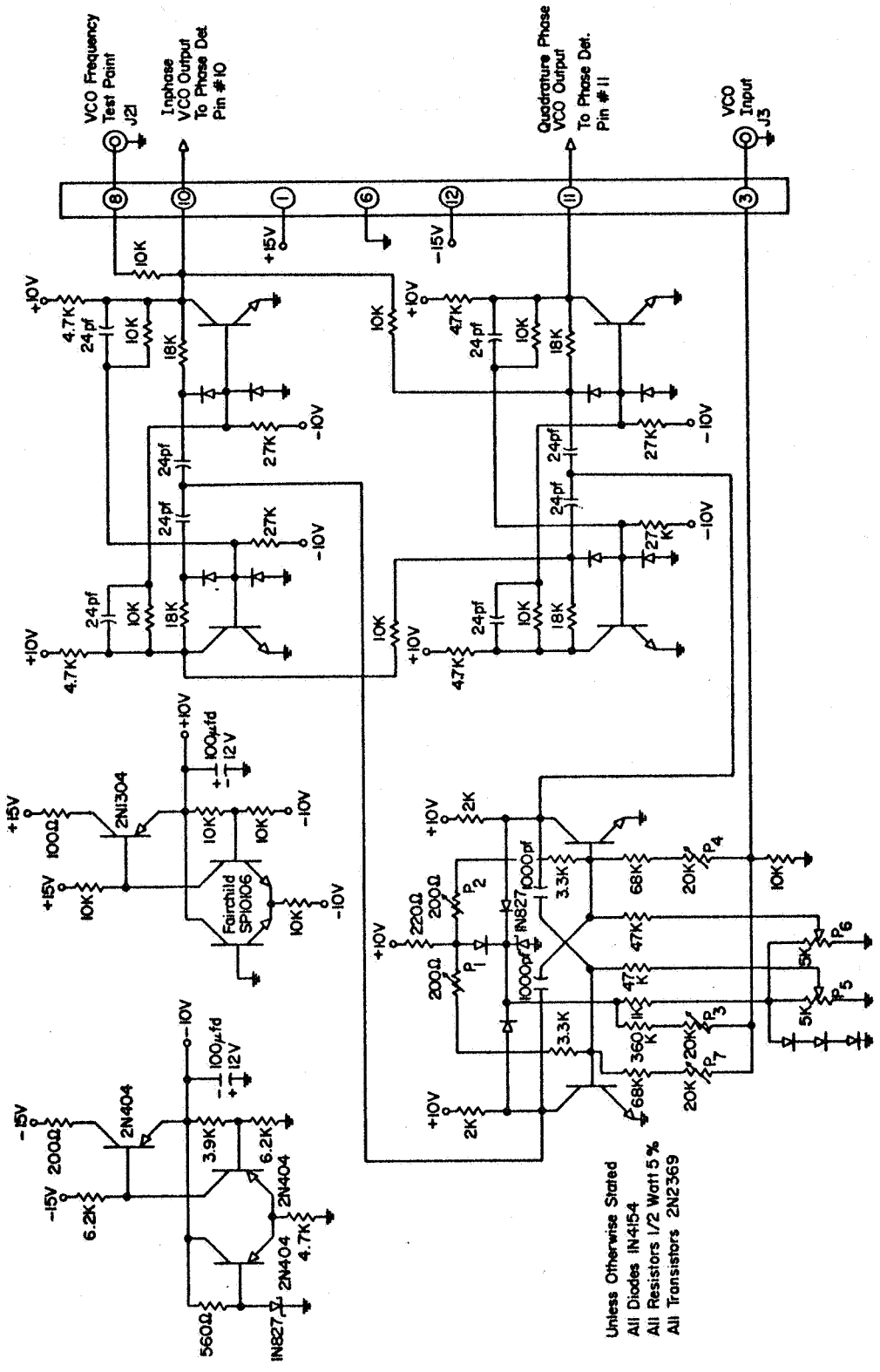


FIGURE B.I. VCO .

comparison of the output, is amplified and fed back as a correction signal. The 1N827 zener diode used for a reference in the negative supply has a very low, 50 ppm, voltage temperature coefficient. High frequency noise and transients are reduced by the 100 μfd capacitors used on each regulator output. All power used within Figure B.1 except for the VCO multivibrator collector clamp is obtained from these two regulators. The VCO collector clamp power is further regulated by the second stage mentioned above. This consists of a 1N827 zener diode.

The VCO signal is generated by a free running multivibrator. The VCO input, J3, controls the frequency by changing the charging current on the two cross coupling capacitors. The potentiometers P_4 and P_7 control the voltage to frequency conversion rate and waveform symmetry. P_3 adjusts the voltage at J3 to zero when there is no connection there. P_5 and P_6 compensate the frequency and waveform symmetry dependence on temperature. P_1 and P_2 control the natural frequency and waveform symmetry. The natural frequency is the frequency when the VCO input is zero.

The VCO collectors are clamped to the 6.2 V zener level by a pair of diodes. This helps improve the frequency stability by establishing a firm logic level. The complimentary VCO outputs are coupled to a pair of flip-flops. These flip-flops function as frequency dividers. However the lower one is gated by the state of the upper so that the state of the upper lags that of the lower by 1/4 of a period. Otherwise the upper could lead the lower which would not be correct. The voltage swing at pins 10 and 11 is nominally from .2 to 5V. These signals are used as the references for the analog gates in the phase detector.

The alignment procedure requires the sequential adjustment of the

seven potentiometers for proper oscillator calibration.

First the input J3 is grounded. Then using an oscilloscope connected to pins 10 and 11 and a counter connected to either pin, the frequency is adjusted to 100 KHz. using equal adjustments of P_1 and P_2. The delay between pins 10 and 11 is adjusted to exactly 1/4 period by using opposite adjustments of P_1 and P_2 such that the frequency is maintained at 100 KHz.

Next J3 is connected to 10 volts and P_3 and P_4 are adjusted in the same manner as P_1 and P_2 for 1/4 period delay and 105 KHz. Because of the interaction of these four potentiometers it is necessary to alternately repeat the adjustment procedure for each pair several times until the desired condition is attainable for both tests without further adjustment.

Then the input to J3 is left unconnected and P_7 is adjusted for zero voltage at J3.

The temperature compensation is corrected by P_5 and P_6. This is done by turning off the VCO power for twenty seconds after it has been operating for one hour. Then the power is turned on and the frequency at pin 10 or 11 is monitored. P_5 and P_6 are in proper adjustment if the frequency change after returning on the VCO power is less than 10 Hz. and the waveforms at pins 10 and 11 remain within .01 radian of being in perfect phase quadrature. Because of interaction it may be necessary to repeat the whole procedure several times.

B.2. The Phase Detector

Figure B.2 is the circuit diagram of the Phase Detector. The phase detector specifications are: 1. the inputs from the VCO, pins 10 and 11,

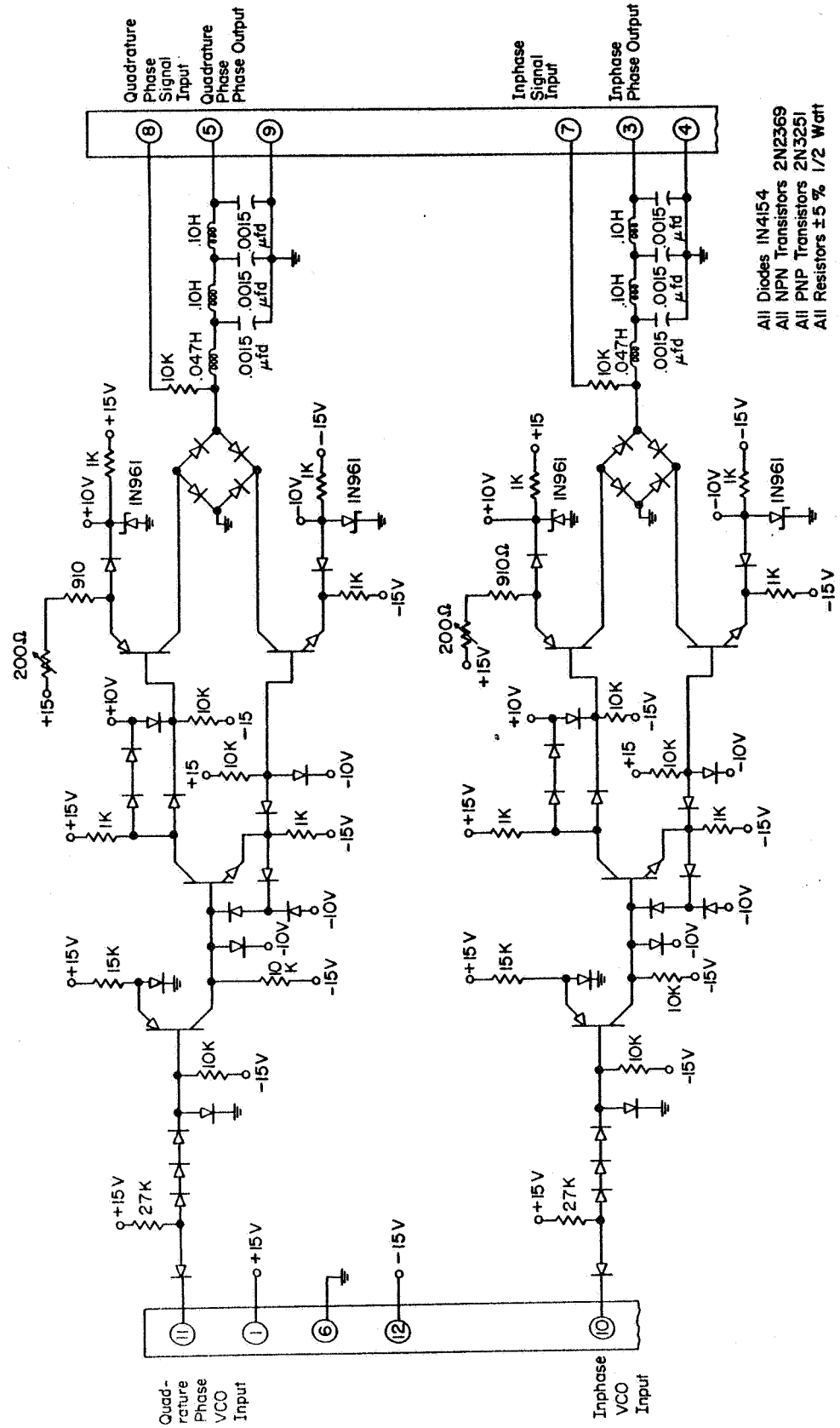


FIGURE B.2. PHASE DETECTOR.

require binary signals with logic levels of < .5 V and > 1.5 V for the "0" and "1" conditions respectively; 2. the isolation provided by each analog gate when closed is greater than 70 db; 3. with zero voltage at pins 7 and 8, the DC offset of each analog gate when closed is less than .1 mv; 4. with 100 KHz. applied to the phase detector from the VCO and 99 or 101 KHz. sinusoidal signal of five volts peak amplitude applied to pins 7 and 8, the DC offset at pins 3 and 5 is less than 5 mv; 5. the LPF at the output of each diode bridge gate provides 70 db attenuation between the frequencies of 90 KHz. and 1 MHz.

The most important parts of the phase detector are the analog gates. The diode bridges used for these gates have to provide sufficient attenuation of the input signal and a small residual DC level when in the on condition and little distortion of the signal when off. Therefore special diodes matched for this purpose and donated by General Electric were used. These gates are switched on and off by a balanced current driver. The amplifier supplying this drive must provide very fast switching of the gate. For this reason current mode logic circuitry is used. The current drive in the two complimentary drivers is balanced by the two 200 Ω potentiometers. These are adjusted so that the DC offset at pins 3 and 5 is less than .1 mv when the signal at pins 7 and 8 is zero and the VCO is at a frequency of 100 KHz.

B.3. The Sin and Cos Phase Inverters

Figure B.3 is the circuit diagram of the Sin and Cos Phase Inverters. The purpose of these blocks is to amplify, invert and filter the phase detector outputs as well as isolate them from the NDG and Zero Crossing Detectors.

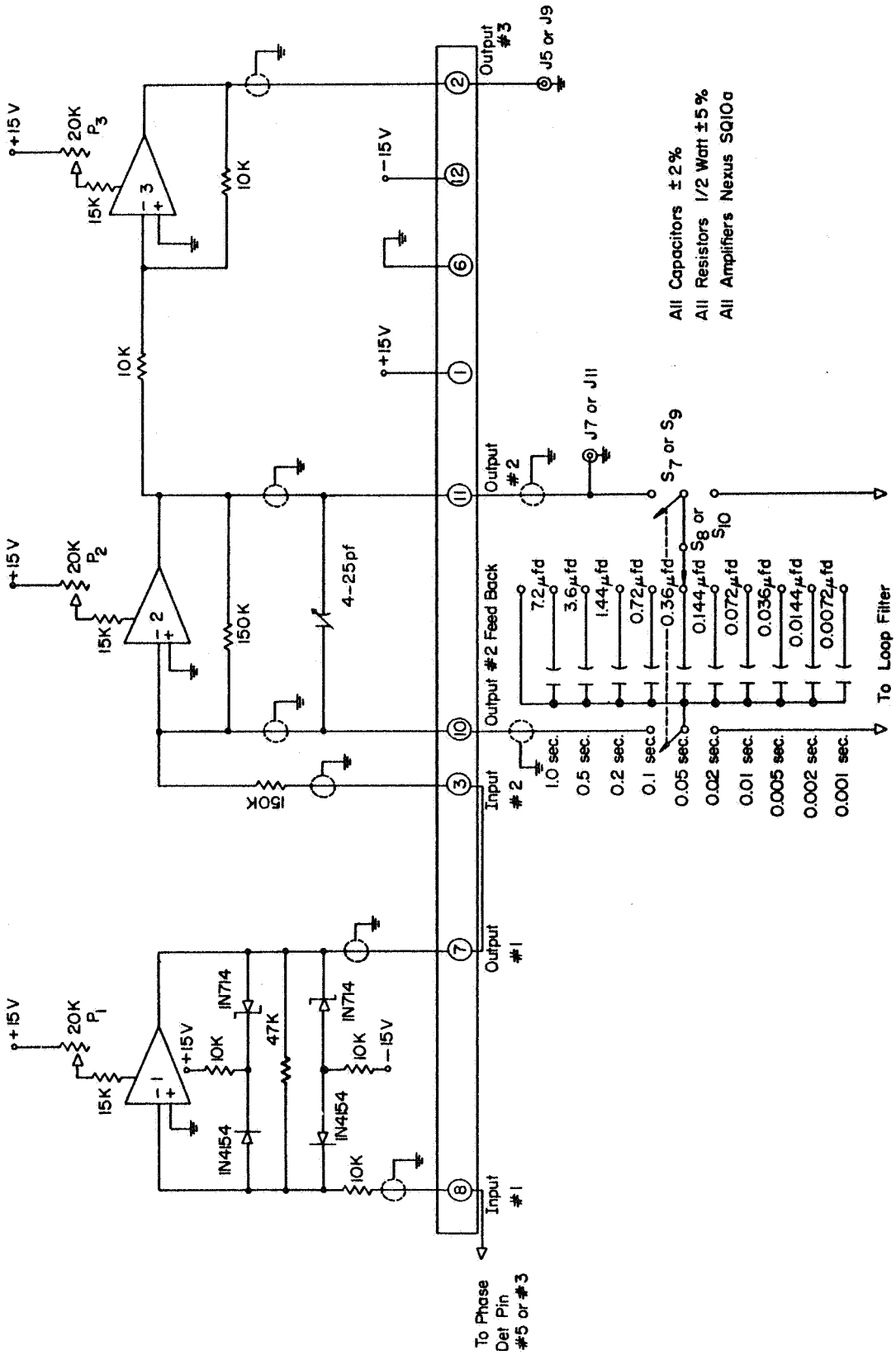


FIGURE B.3. SIN AND COS PHASE INVERTERS.

The first amplifier is used as an isolator and as a current load for the diode gates in the phase detector. The diode feedback network is used to prevent the amplifier from saturating and limits the output swing to ± 10 V. The gain of the amplifier is set by the 47 K resistor so that the maximum signal voltage at pin 7 is the same as that at the phase detector input. Under this condition the voltage at pin 7 is

$$e_7 = A \, \mathrm{Sin}[(\omega_c - \omega_v)t + \phi(t) - \theta(t)] + 2n(t) \, \mathrm{Cos}[\omega_v t + \theta(t)]. \qquad (B.1)$$

The second amplifier is connected as a first order LPF. The time constant is controlled by the front panel switches S_8 and S_{10} for the Sin and Cos filters respectively. The double pole double throw switches S_7 and S_9 make it possible to measure the capacitance value of the LPF capacitor at J48 on the system back panel. These switches are located on the system back panel. When these switches are in the center off position the amplifier roll-off is controlled by the 4 - 25 pf capacitor. This capacitor is adjusted to equalize the delay of the Sin and Cos Phase Inverters and to control the amplifier overshoot.

The third amplifier is used to provide the inverted phase detector output. The inphase and quadrature phase detector outputs as well as their inverses are brought to J5, J7, J9, and J11 on the system front panel.

The only alignment necessary is the balancing of the three operational amplifiers with P_1 through P_3 respectively.

B.4. The Sin and Cos Zero Crossing Detectors

Figure B.4 is the circuit diagram of the Sin and Cos Zero Crossing Detectors (ZCD). The purpose of these circuits is to determine the sign of the two phase detector outputs. Each generates a binary signal at pin

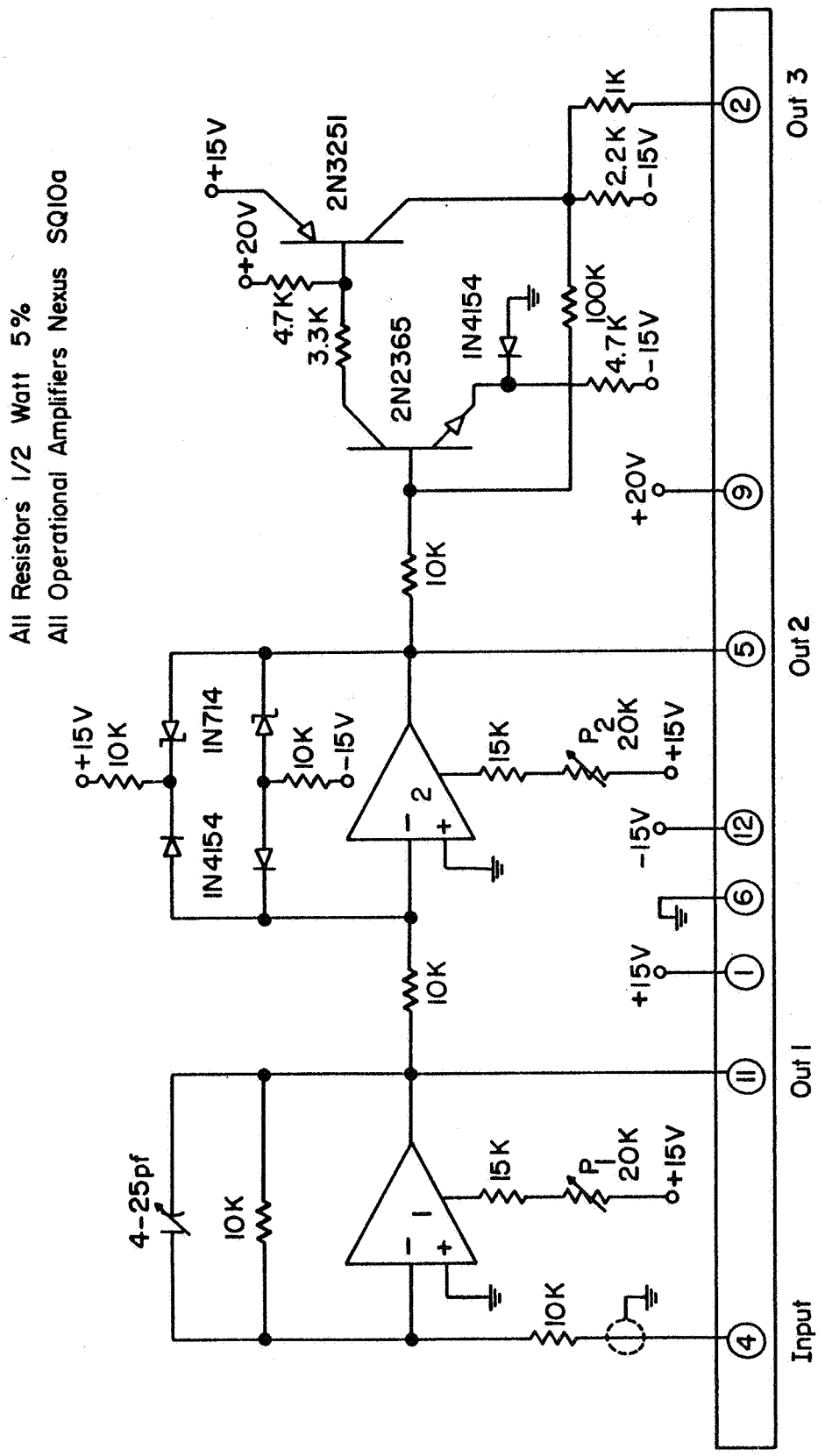


FIGURE B.4. SIN AND COS ZERO CROSSING DETECTORS.

2 depending on the sign of the signal at pin 4.

The first operational amplifier provides isolation of the phase inverter output from the ZCD. The 4 - 25 pf capacitor controls the delay and roll off of the ZCD. The second amplifier is operated essentially without feedback. The only feedback is a diode network that limits the output signal to $\pm$ 10 V. When the output is not limiting the amplifier gain is in the order of 100 db. This causes the amplifier to function effectively as a ZCD.

The complementary schimtt driven by the second amplifier generates a binary signal which changes state when the ZCD input passes through zero.

The alignment consists of adjusting the delay and balance of the two amplifiers.

B.5. The Numerator and Denominator Generator

Figure B.5 is the circuit diagram of the NDG. The purpose of the NDG is to provide the signals

$$e_N = A[\mathrm{Sin}\phi_B \ \mathrm{SGN}(\mathrm{Cos}\phi_B) - \mathrm{Cos}\phi_B \ \mathrm{SGN}(\mathrm{Sin}\phi_B)] \qquad (B.2)$$

and

$$e_D = A[|\mathrm{Sin}\phi_B| + |\mathrm{Cos}\phi_B|]. \qquad (B.3)$$

The diode gates are the most important part of this circuit. They are selected and matched for offset voltage and capacitance. P_1 through P_8 are adjusted under zero signal input and closed gate condition so that the bridge offset is less than 1 mv.

The NDG specifications are: 1. the offset voltage with any signal less than 10 volts and a closed bridge is less than 10 mv; 2. the attenuation of each gate when closed is greater than 60 db.

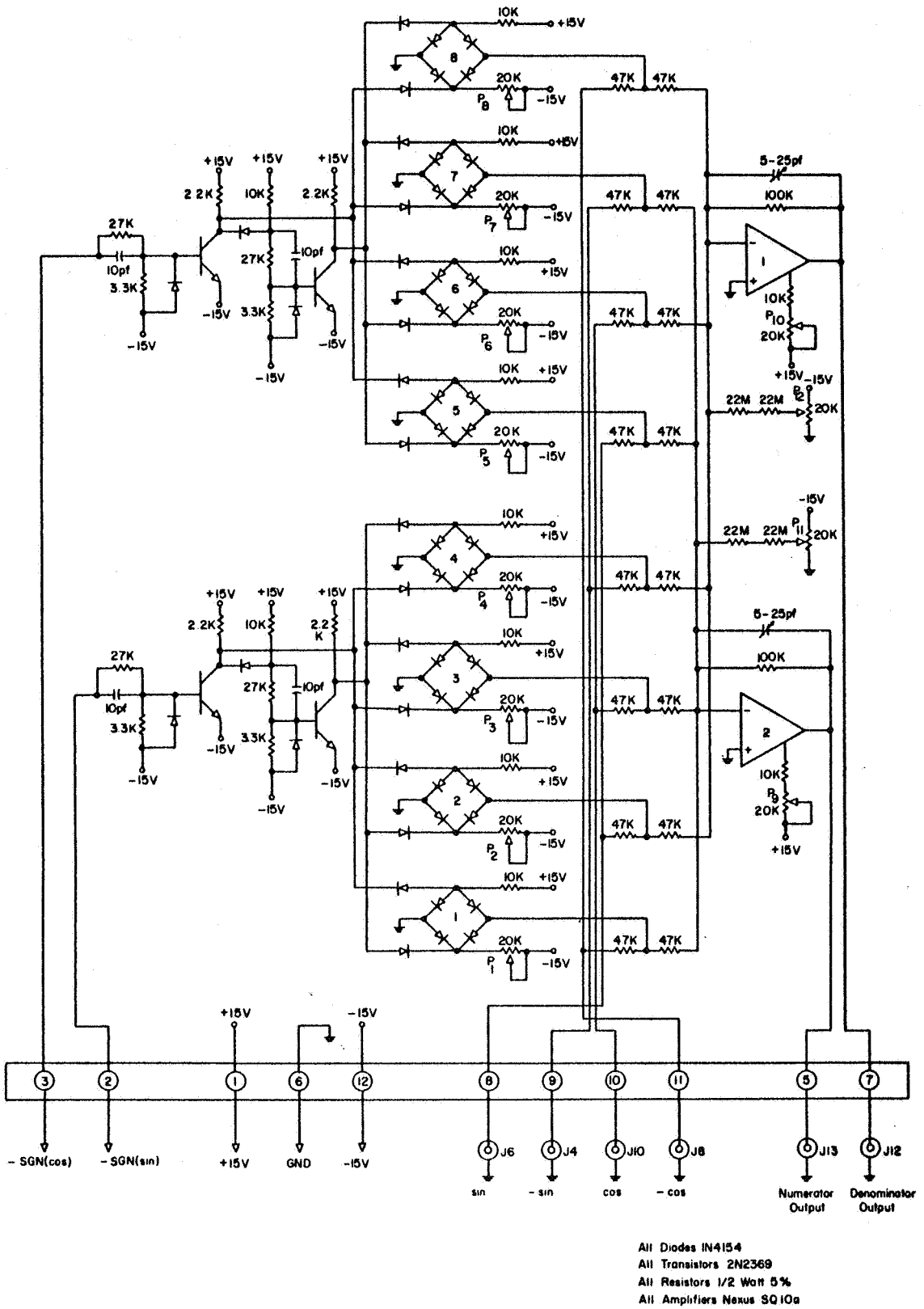


FIGURE B.5. NUMERATOR AND DENOMINATOR GENERATOR.

The binary control signals are amplified by the transister circuits on the left and phase split so as to provide balanced voltage drive for the analog gates.

The outputs of the gates are summed by the operational amplifiers. The potentiometers P_9 and P_{10} compensate for the amplifier offset voltage. P_{11} and P_{12} compensate for the amplifier input offset current.

The alignment procedure requires that P_1 through P_8 be adjusted for zero gate output voltage. The amplifier is balanced by simultaneously adjusting the input and output voltage of each amplifier using P_9 through P_{12}. Because of the potentiometer interaction it may be necessary to repeat the procedure several times.

The two NDG outputs J12 and J13 are routed to the Philbrick Analog Divider. The output of the divider is the tangent of the phase error modulo $\pi/2$.

B.6. The Arc Tangent Converter

Figure B.6 is the circuit diagram of the Arc Tangent Converter. The purpose of this circuit is to provide an Arc Tangent non-linear transfer function over a range of $\pm \pi/4$. The desired transfer function is given by

$$e_{out} = \mathrm{Tan}^{-1}[e_{in}/10]/10^3\ C_1,\ |e_{in}| < 10\ , \qquad (B.4)$$

where $C_1 = 1/K$. This function is approximated by a 7 segment piecewise linear approximation. The break points are adjusted by P_1 through P_6. The slopes are set by P_{10} through P_{15} and P_7. The accuracy of the approximation was checked and found to be accurate to within $\pm$ .02 radian.

The loop gain, K, is controlled by S_{11} over a range of 10 to 10^4. This is done by changing the feedback resistor on the operational

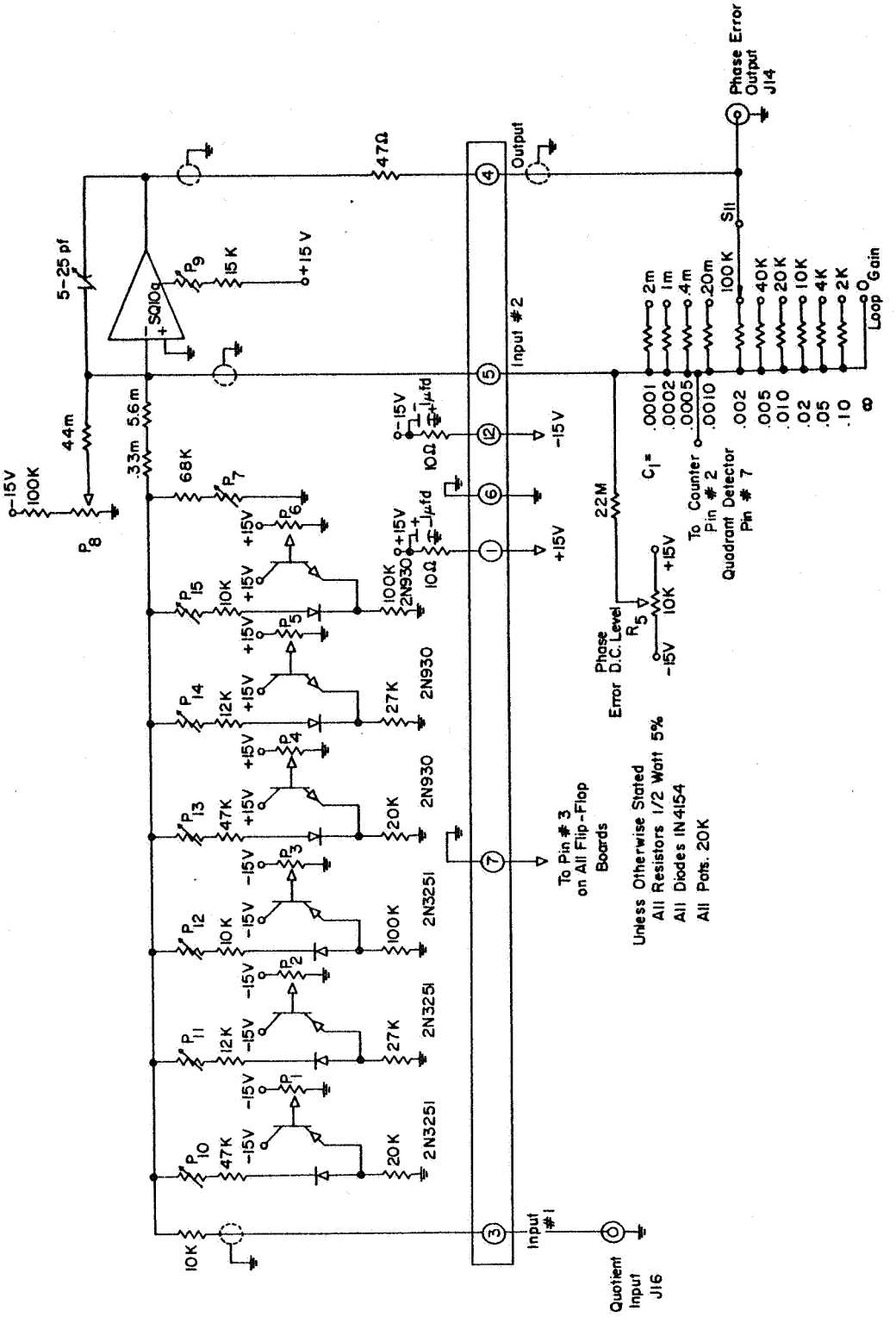


FIGURE B.6. ARC TANGENT CONVERTER.

amplifier. The amplifier input is used as a summing point for the three parts of the phase error current. Currents proportional to the quadrant from the Quadrant Detector and the number of cycles slipped from the 10 Bit Counter are added to that due to the modulo $\pi/2$ phase error at pin 5. Pin 7 is the ground return for these currents. The output at J14 is proportional to the modulo $2N\pi$ phase error, Φ_e.

This amplifier is balanced for both voltage and current offset by P_9 and P_8 respectively. R_5 is a front panel control used to compensate for DC error in the D/A converter output.

Table B.1

Arc Tangent Non-linearity Alignment Procedure

Step	e_{in}(volts)	e_{out}(volts)	Potentiometer Adjustment
1	-1.57	.5	P_7
2	-3.14	.97	P_1
3	-5.0	1.48	P_{10}
4	Repeat steps 2 and 3		
5	-6.5	1.84	P_2
6	-8.0	2.15	P_{11}
7	Repeat steps 2 through 6		
8	-9.0	2.34	P_3
9	-10.0	2.5	P_{12}
10	Repeat steps 2 through 9		
11	3.14	- .97	P_4
12	5.0	-1.48	P_{13}
13	Repeat steps 11 and 12		
14	6.5	-1.84	P_5
15	8.0	-2.15	P_{14}
16	Repeat steps 11 through 15		
17	9.0	-2.34	P_6
18	10.0	-2.5	P_{15}
19	Repeat steps 11 through 18		

To align this circuit it is necessary to set the arms of P_1 through P_6 to maximum voltage magnitude. The input at J16 is grounded. The arm

of R_5 is set in the center of its range and grounded. P_8 and P_9 are adjusted alternately to balance the amplifier. Table B.1 gives input/output voltages required and the order of making adjustments for the nonlinearity. For these adjustments C_1 = .0001.

Because of the interaction between the adjustments and the degree of accuracy required, it may be necessary to repeat steps 1 - 19 several times in order to verify that each step is attainable without further adjustment of P_1 - P_7 and P_{10} - P_{15}.

B.7. The N Selector Switch

Figure B.7 is the circuit diagram of the N Selector Switch. The purpose of the N Selector Switch is to set the value of the phase error range factor, N. The phase error range is $2N\pi$ radians. The N Selector Switch generates signals that are used to control the 10 Bit Counter and Quadrant Detector. The switch S_{33} has its positions labeled - 1 through 11. The correspondence between N and this number, L, is

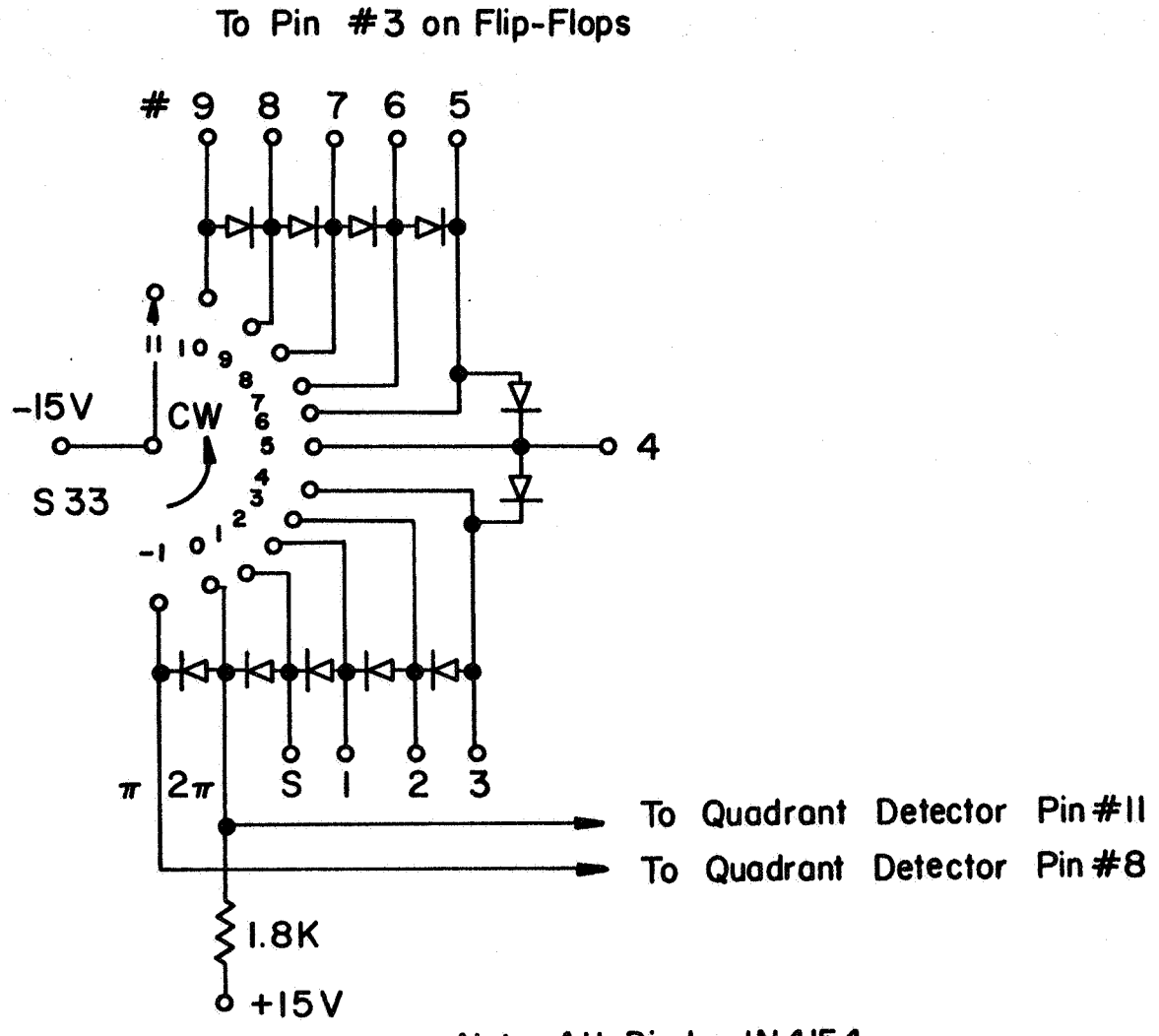
$$N = 2^{L} - 1 \qquad (B.5)$$

or in other words the phase error range is $2^{L}\pi$ radians.

This circuit places negative control voltages on all flip-flops in the counter that are not needed for a particular value of N and a similar control voltage labeled π and 2π are available for the Quadrant Detector. The numbers 1 through 9 on the external switch connections go to pin 3 on the first nine flip-flops of the counter. The terminal labeled S goes to the sign or last flip-flop of the counter.

B.8. The Quadrant Detector

The purpose of the Quadrant Detector is to generate a current



Note: All Diodes IN4154

FIGURE B.7. N SELECTOR SWITCH.

depending on the quadrant of the modulo 2π phase error such that the sum of the modulo $\pi/2$ phase and the Quadrant Detector output yields a signal proportional to the modulo 2π phase error for $N \geq 1$,

$$(\phi_B + \pi)_{\text{Mod } 2\pi} - \pi = \phi_Q + (\phi_B + \pi/4)_{\text{Mod } \pi/2} - \pi/4, \tag{B.6}$$

and one proportional to the modulo π phase error for $N = .5$,

$$(\phi_B + \pi/2)_{\text{Mod } \pi} - \pi/2 = \phi_Q + (\phi_B + \pi/4)_{\text{Mod } \pi/2} - \pi/4. \tag{B.7}$$

For $N = .25$, $\phi_Q = 0$. ϕ_Q is the quadrant phase factor. The phase coefficient of the current summing junction of the Arc Tangent Converter is - 1 μamp/2π radian phase error. Table B.2, which is derived from (B.5) and (B.6), gives the quadrant factor current i_Q as a function of N and the quadrant number.

Table B.2

i_Q (μamps) Versus N and the Quadrant Number

$\phi_e \mid_{\text{Mod } 2\pi}$ Quadrant	N .25	.5	≥ 1
1	0	-.25	-.25
2	0	.25	-.75
3	0	-.25	.75
4	0	.25	.25

Figure B.8 is the circuit diagram of the Quadrant Detector. It generates an output current at pin 5 according to the schedule in Table B.2. The quadrant number is determined from the $SGN(Sin\phi_B)$ and $SGN(Cos\phi_B)$ and the π and 2π control signals from the N Selector Switch.

This table is implemented in the circuit by 4 logic controlled current generators of - .5, - .25, .25 and .5 μamps. Each is independently

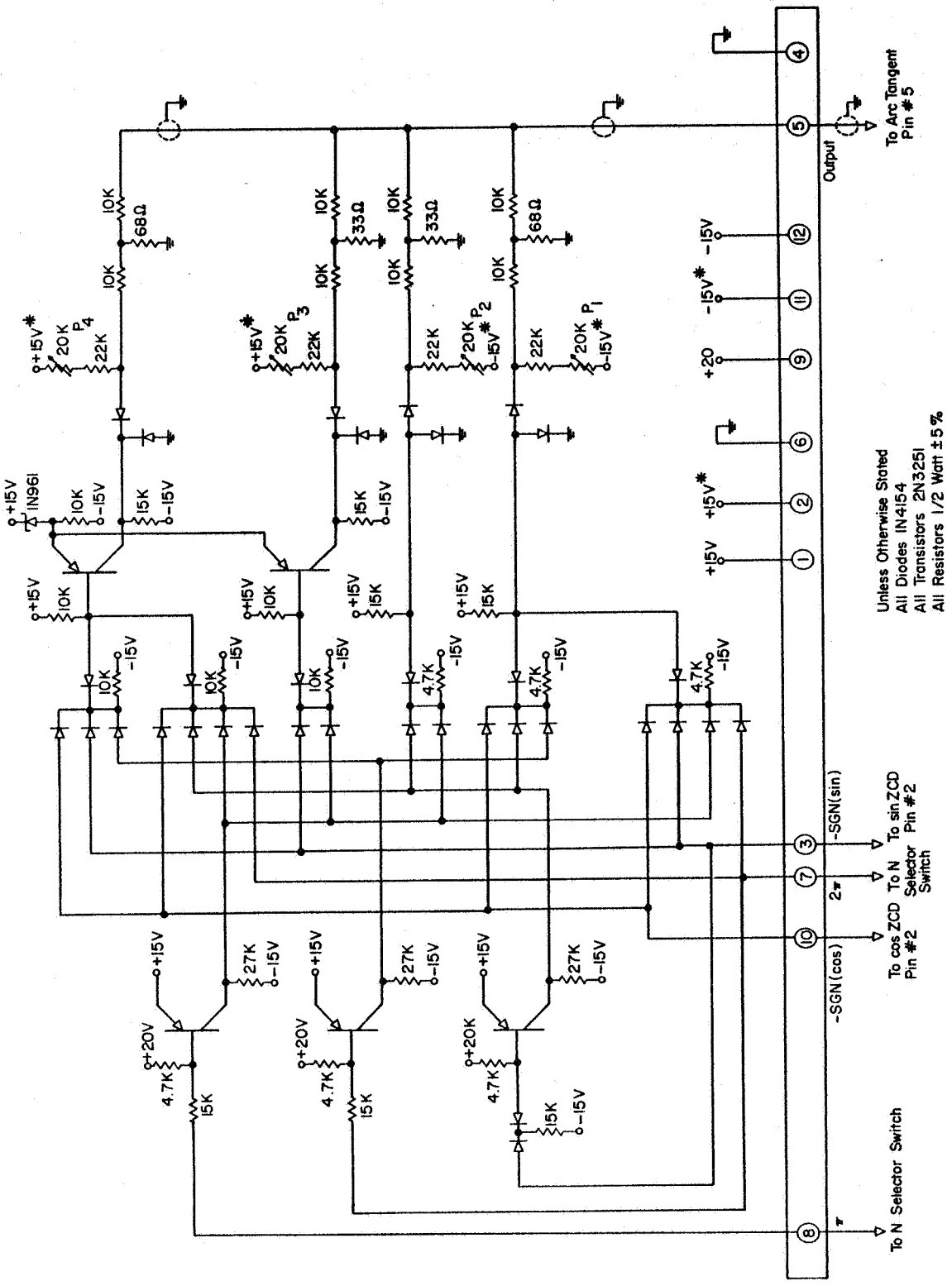


FIGURE B.8. QUADRANT DETECTOR.

calibrated by P_1 through P_4 respectively. The output, pin 5, is summed with the other two phase error information signals at pin 5 of the Arc Tangent Generator.

B.9. The Cycle Slip Detector

The purpose of the Cycle Slip Detector is to generate a subtract pulse whenever a negative 2π radian cycle slip occurs and an add pulse whenever a positive 2π radian cycle slip occurs. A cycle slip occurs whenever the modulo 2π phase error passes through zero. The direction of the pass is the direction of the cycle slip.

Figure B.9 is the circuit diagram of the Cycle Slip Detector. The blocking oscillator (B.O.) generates a 5 μsecond pulse each time the input at pin 11 switches from -5 V to 15 V or 15 V to -5 V.

If the first transition of the signal at P_{11} occurs while the input at pin 2 is negative a subtract pulse is generated at pin 8. If the second transition occurs while the input at pin 2 is negative an add pulse occurs at pin 4.

The specifications on these pulses are that they be between 2 and 6 μseconds in length and have a minimum voltage swing of 10 V to -5 V and back during one pulse duration.

B.10 The Counter

The purpose of the counter is to count the modulo N total of the number of positive cycles slipped minus the number of negative cycles slipped. It generates an analog signal related to this total. This signal must be such that when it is added to the modula 2π phase error the result is the modulo $2N\pi$ phase error. Since a binary counter is used

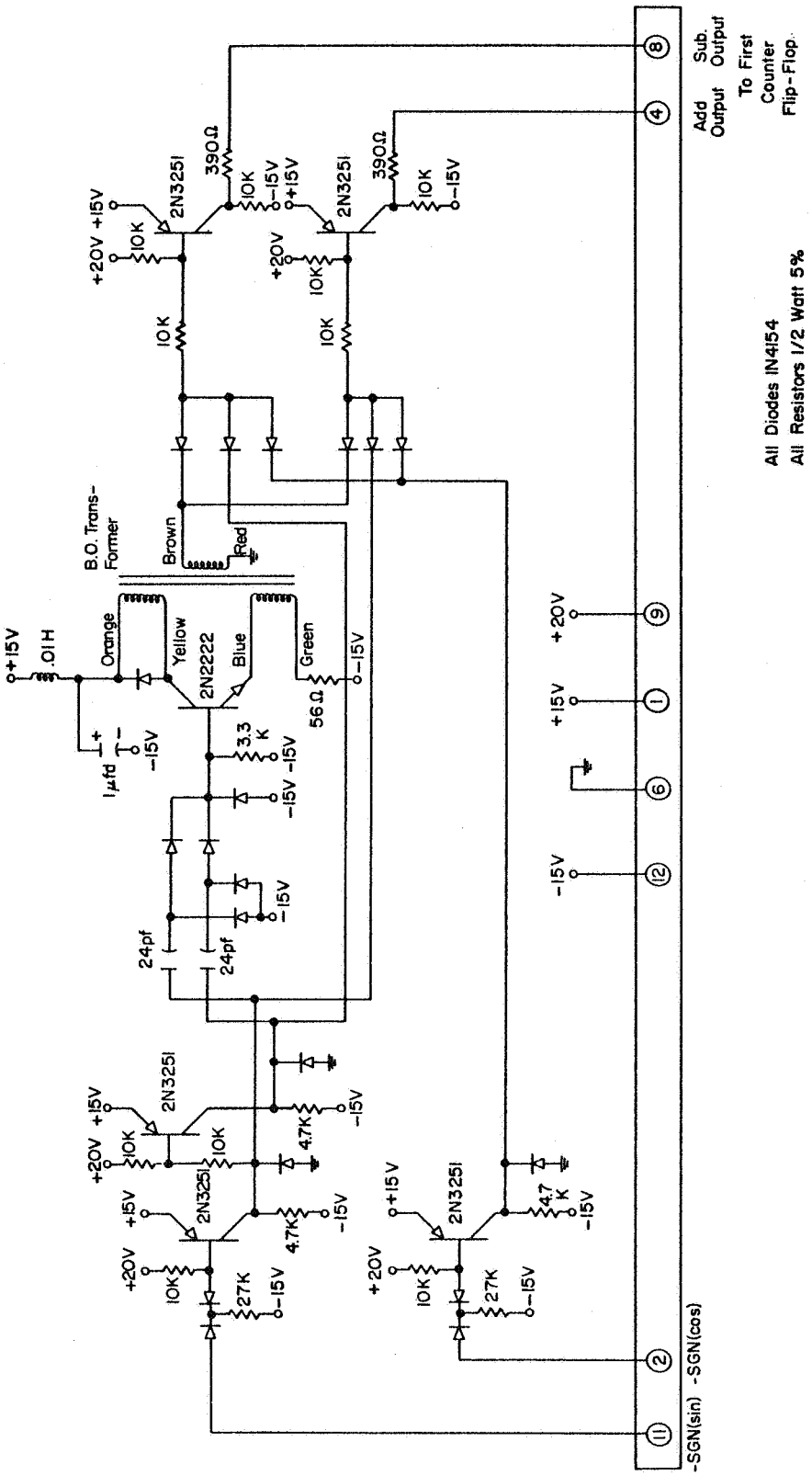


FIGURE B.9. CYCLE SLIP DETECTOR.

it is convenient to limit N to numbers that are powers of 2, such as 1, 2, 4, 8, ··· , 1024. 10 is the maximum number of bits used. Therefore N is bounded by 1024. Since it is desirable for the phase detector characteristic to be symmetric about zero, for $N \geq 1$ the point $\phi_e = 0$ is one boundary point for a 2π radian cycle slip. This somewhat complicates the D/A converter as well as the interrelationships between the first nine flip-flops and the sign flip-flop.

The output current in μamps is given by

$$i_C = - [N_1 + (N - 1)/2]_{\text{Mod } N} + N/2, \qquad \text{(B.8)}$$

where N_1 is the total number of cycles slipped. Thus when no cycles have slipped the output current is .5 μamps, when 1 positive cycle has slipped the output current is - .5 μamps and when 2 positive cycles have slipped the output current is - 1.5 μamps.

Figures B.10 and B.11 are circuit diagrams of the flip-flops used in the 10 Bit Counter. The counter consists of 10 flip-flops. Figure B.10 is the circuit diagram for the first nine flip-flops and Figure B.11 is the circuit diagram for the 10th or sign flip-flop.

Each flip-flop consists of trigger gating and steering circuitry, a binary element (the two cross coupled 2N2369 transistors), the logic level amplifiers (the 2N3251 transistors), a delay feedback for the input trigger steering (the 2N030 transistors) and a D/A converter with sign control logic (the lower right hand corner of the circuit).

In order to reduce the counter propagation delay, gated triggering is used. This means that a trigger pulse for the jth flip-flop appears only if the previous state of the first j - 1 flip-flops is "1" for add pulses or "0" for subtract pulses. With this type of triggering the

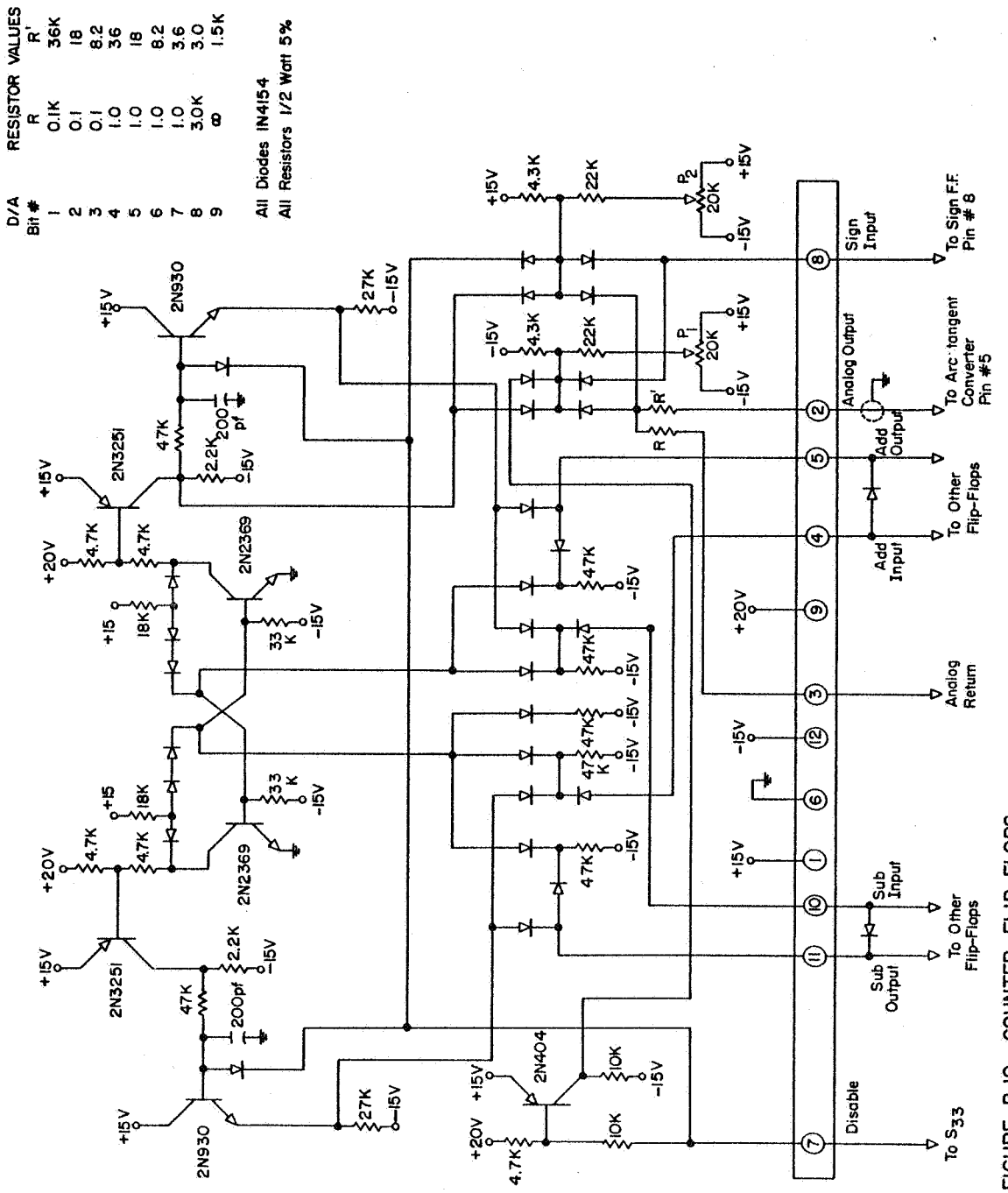


FIGURE B.10. COUNTER FLIP-FLOPS.

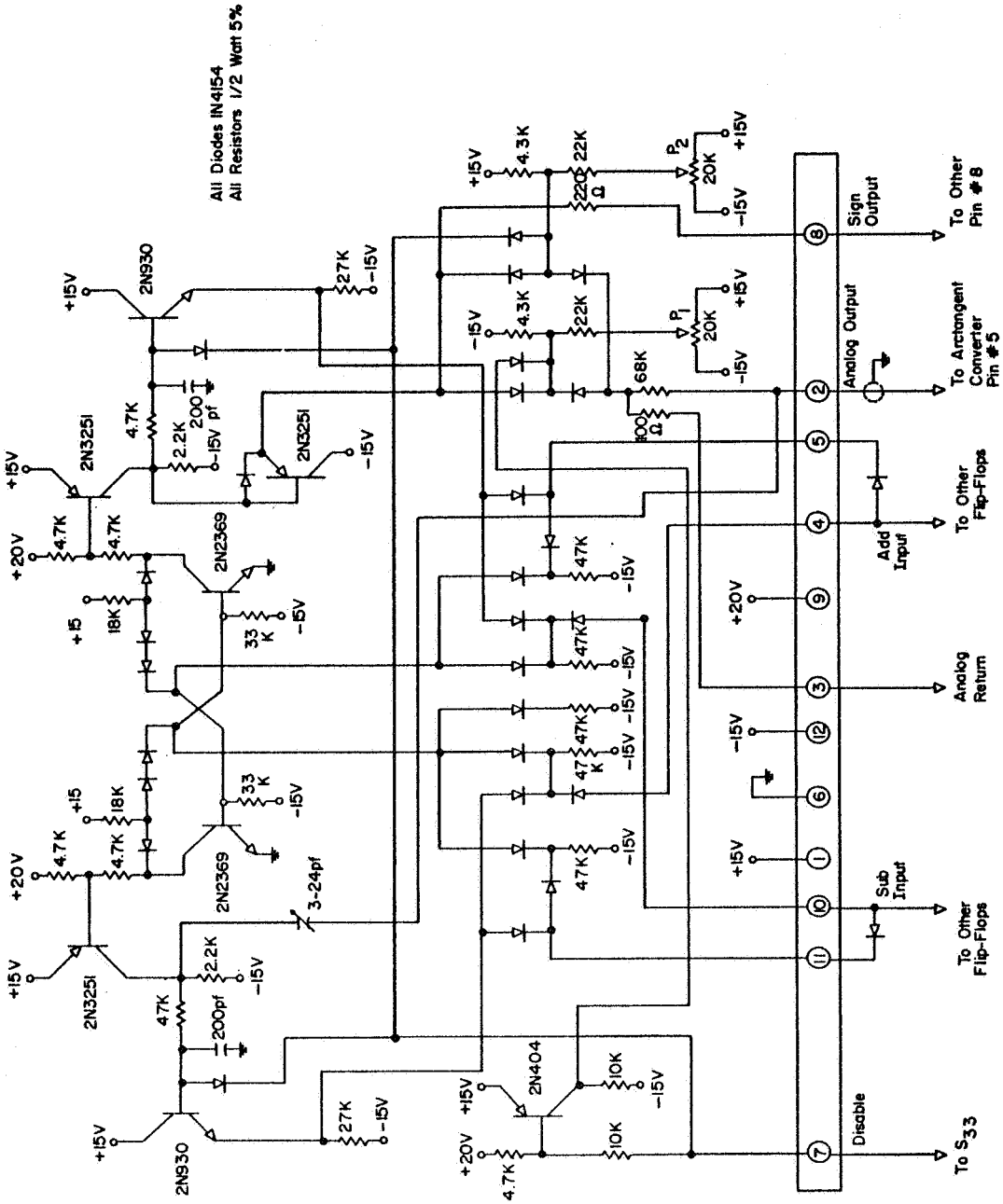


FIGURE B.11. COUNTER SIGN FLIP-FLOP.

trigger delay for the jth flip-flop is only dependent on the delay of j diodes rather than the delay of j - 1 flip-flops. The latter in general is an order of magnitude greater.

In order to improve the switching time of the flip-flops and increase the range of acceptable trigger levels, pulse widths and rise times, DC triggering with delayed feedback gating is used. The delay in the base circuit of each 2N930 transistor has a time constant of 10 μseconds. Therefore the trigger steering gate does not know that the flip-flop has switched state until 10 μseconds afterwards. By this time the trigger pulse has terminated and the possibility of an ambiguity or double trigger is eliminated.

The disable input, pin 7 from the N Selector Switch, causes the trigger pulses to by-pass the flip-flop and disables the D/A converter output. The D/A converter generates a current i_{cj} for the jth flip-flop given by

$$i_{cj} = \begin{cases} 2^j \text{ if } SGN(N_2) < 0 \text{ and } FF_j \text{ in "zero" state} \\ -2^j \text{ if } SGN(N_2) \geq 0 \text{ and } FF_j \text{ in "one" state} \\ 0 \text{ otherwise,} \end{cases} \qquad (B.9)$$

where $N_2 = [N_1 + N/2]_{Mod\ N} - N/2$.

The resisters R and R′ control the current level in a gross way. The two 20K potentiometers, P_1 and P_2, are for calibrating the negative and positive currents respectively. The current return, pin 3, for the current divider, R and R′, is necessary to minimize the effect of contact resistence in the circuit board plug.

The tenth flip-flop in Figure B.11 is the sign flip-flop. It only changes state when the count passes from 0 to - 1 in either direction or

when the counter overflows in either direction. The major difference between B.11 and B.10 is that the former has a 2N3251 emitter follower to provide a low impedance logic output at pin 8 for the "sign" logic signal that is used by the other flip-flops in the counter. Also the D/A output is compensated for overshoot by the 3 - 24 pf capacitor.

B.11 The Loop Filter

The purpose of the loop filter is to control the loop transfer function. Figure B.12 is the circuit diagram of the loop filter. Only the items above the connector are on the circuit board. The first three operational amplifiers are connected as integrators, the fourth as a fixed gain summer and the fifth as a variable gain summer controlled by R_1.

The time constant of the first integrator is controlled by S_2, that of the second by S_4 and that of the third by S_6. The switches S_1, S_3 and S_5 connect the timing capacitor of the respective integrator to J48, the back panel monitoring point, so that each capacitor can be measured to calibrate the time constant. The resistors R_2 through R_4 control the fine adjustment of the time constants. The resistor R_1 provides fine adjustment of the loop gain K together with S_{11} of the Arc Tangent circuit.

The relays RL_2 through RL_4 are used to "hold" the conditions of the loop filter. This is done by disconnecting the inputs to the integrators. Under this condition the drift of the integrator is limited by the offset current which is in the order of 100 picoamps. The offset current is compensated by an adjustment in the initial condition controller. This adjustment brings the maximum offset current to less than 10 picoamps. The

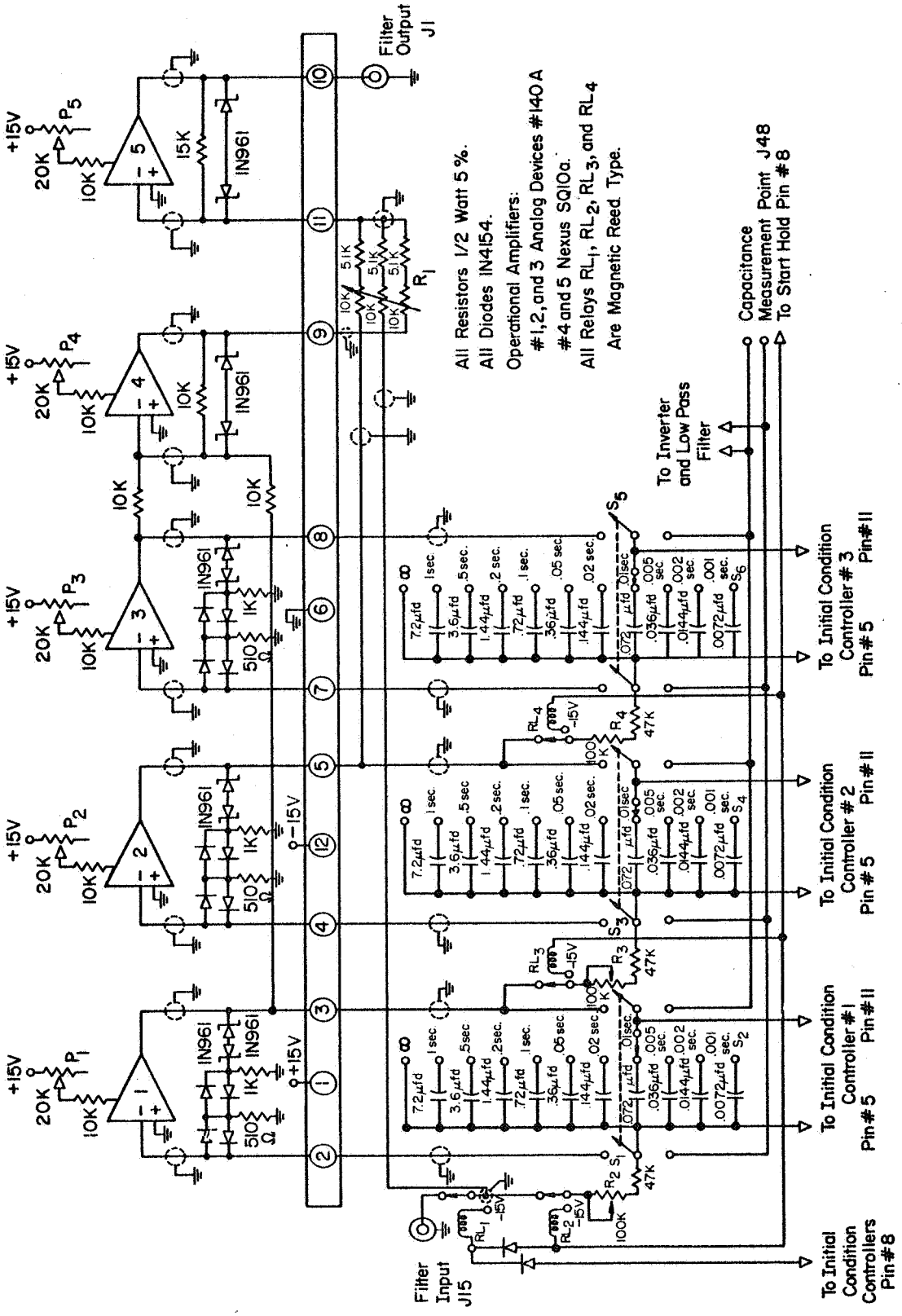


FIGURE B.12. LOOP FILTER

control circuitry for the hold relays is discussed in Appendix D.

The initial conditions for the three integrators are determined by the three initial condition controllers. Each integrator can be independently set to any initial condition between ± 10 volts.

The only alignment procedure necessary for the loop filter is the adjusting of P_1 through P_5 to balance the operational amplifier offset voltage.

B.12. The Initial Condition Controller

Figure B.13 is the circuit diagram of the Initial Condition Controller. Three of these circuits are used to set the initial conditions of the three integrators.

The initial condition voltage is set by R_{15} - R_{17}. This voltage can be monitored at the S_{30} output jack, J44. When the initial condition is applied it can also be monitored at the integrator output jacks, J29, J30 and J31. P_2 adjusts the integrator offset current compensation. This is held to within 10 picoamps in this manner.

B.13. The Front Panel and Control Lists

Figure B.14 is the front panel layout of the ELRPLL. Table B.3 is a list of the connectors or J numbers. Table B.4 is a list of the switches of S numbers. Table B.5 is a list of the front panel variable resistor or R numbers and variable capacitor or C numbers.

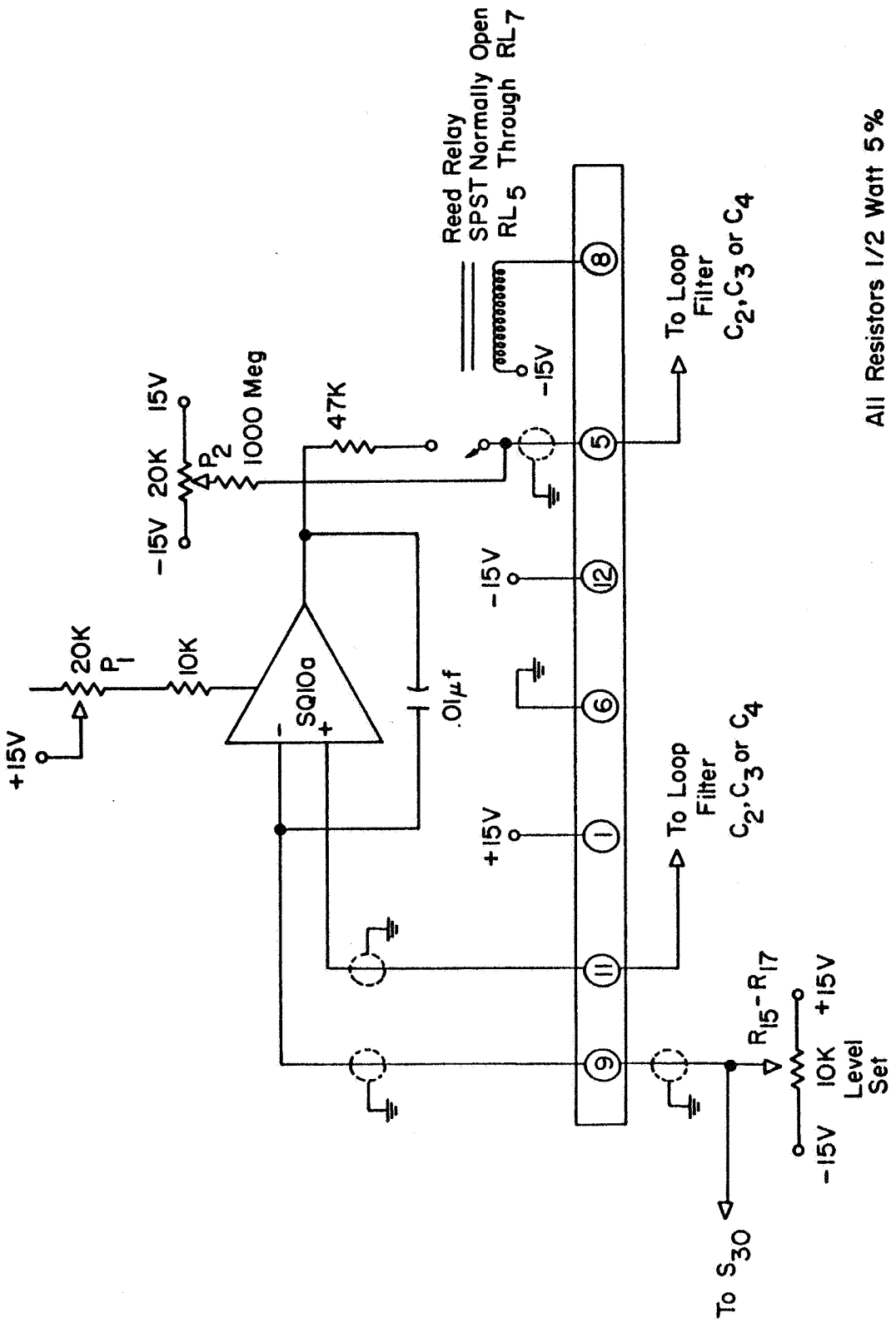


FIGURE B.13. INITIAL CONDITION CONTROLLER.

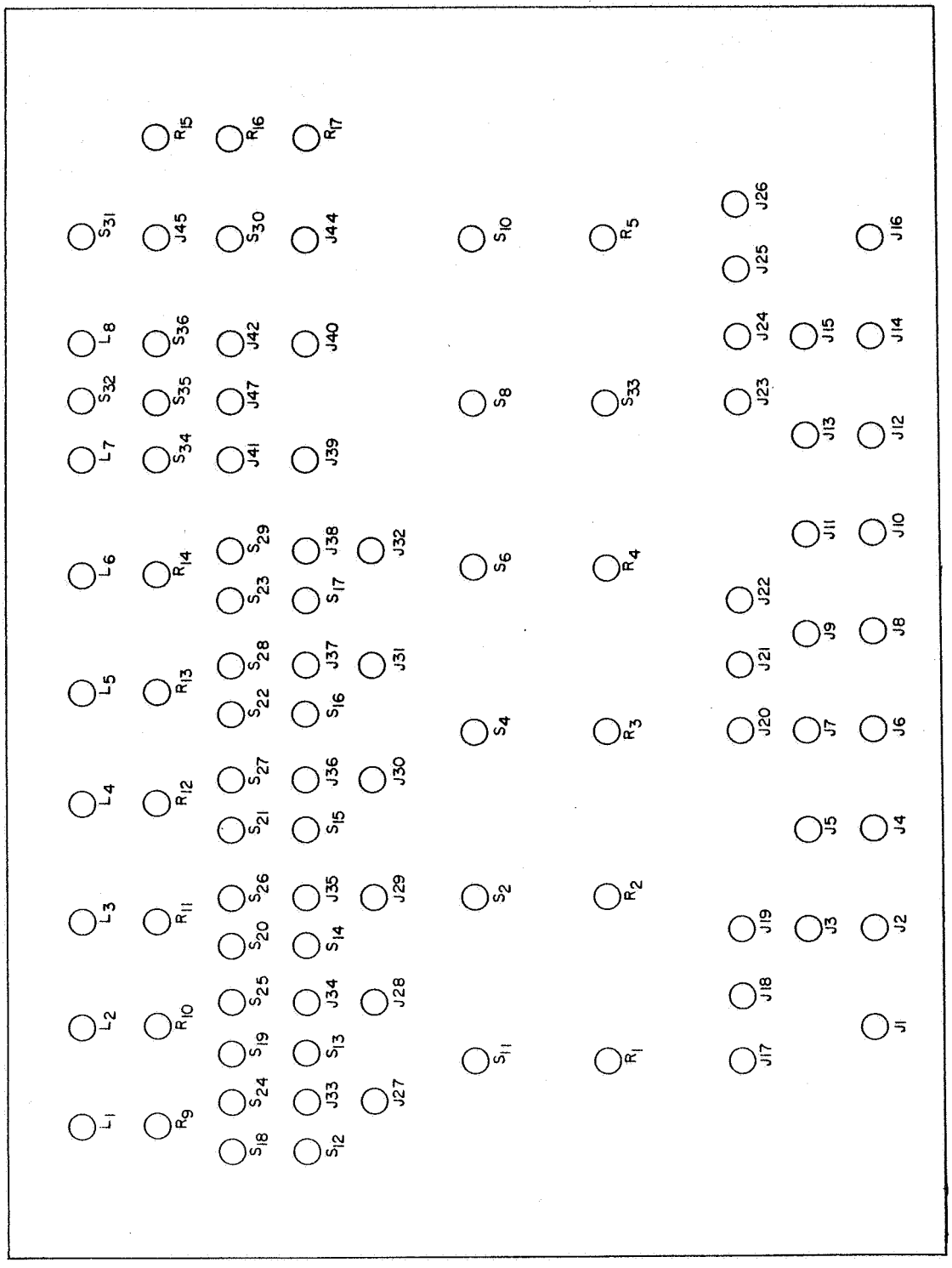


FIGURE B.14. FRONT PANEL LAYOUT FOR ELRPLL AND LOOP CONTROL SYSTEM.

Table B.3

List of External Connectors

J Number	Purpose
1	Filter output
2	Signal input
3	VCO input
4	- Sin phase error input
5	- Sin phase error output
6	+ Sin phase error input
7	+ Sin phase error output
8	- Cos phase error input
9	- Cos phase error output
10	+ Cos phase error input
11	+ Cos phase error output
12	Denominator output
13	Numerator output
14	Phase error output
15	Filter input
16	Quotient input
17	Sin phase error
18	VCO input
19	SGN(Sin)
20	Cos phase error
21	VCO frequency
22	SGN(Cos)
23	+ 20 V
24	+ 15 V
25	- 15 V
26	Ground
27	Filter output
28	Phase error
29	C_2 voltage
30	C_3 voltage
31	C_4 voltage
32	Blank
33	Level detector no. 1 input
34	Level detector no. 2 input
35	Level detector no. 3 input
36	Level detector no. 4 input
37	Level detector no. 5 input
38	Level detector no. 6 input
39	Start input
40	Hold input
41	Start output
42	Hold output
43	S_{31} output
44	S_{30} output
45	Power plug

Table B.3. Continued

J Number	Purpose
47	Logic output
48	Capacitance value monitor
49-50	Auxiliary amp inputs
51-52	Auxiliary amp outputs
53	Amp-Filter no. 1 input
54	Amp-Filter no. 1 output
55	Local oscillator for mixer input
56	Mixer signal input
57	Amp-Filter no. 2
58	Threshold test fixture output 2
59	Threshold test fixture output 1
60	Signal frequency output
61	Modulation input
62	Noise input
63	Auxiliary signal input
64	Signal plus noise output
65	Signal plus noise output
66	Threshold test fixture modulation input
67	Threshold test fixture demodulation input

Table B.4

List of Switches

S Number	Function
1	C_2 disconnect
2	C_2 set value
3	C_3 disconnect
4	C_3 set value
5	C_4 disconnect
6	C_4 set value
7	Sin filter disconnect
8	Sin filter set value
9	Cos filter disconnect
10	Cos filter set value
11	C_1 set value
12-17	Threshold width
18-23	Upper/both/lower
24-29	Hold/start
30	Monitor switch
31	Monitor switch
32	Controller mode
33	Counter range

Table B.4. Continued

S Number	Function
34	Start master
35	S/H reset
36	Hold master
37	ELRPLL power switch
38	Signal generator switch
39	Gain control on auxiliary amplifier
40	Measurement mode
41	Signal level attenuator
42	Noise level attenuator
43	Modulation level attenuator

Table B.5

List of Potentiometers and Capacitors

Number	Function
R_1	Fine adjustment for first filter coefficient
R_2	Fine adjustment for second filter coefficient
R_3	Fine adjustment for third filter coefficient
R_4	Fine adjustment for fourth filter coefficient
R_5	DC adjustment for phase error
R_6	DC balance on output auxiliary amplifier
R7	DC balance on output auxiliary amplifier
R_8	Modulation balance
R_9-R_{14}	Level detector level set
R_{15}-R_{17}	Initial condition set
C_1	Course adjustment for first filter coefficient
C2	Course adjustment for second filter coefficient
C_3	Course adjustment for third filter coefficient
C_4	Course adjustment for fourth filter coefficient

Figure B.15 is the circuit diagram of the ELRPLL, Signal Generator and Channel Power Distributor. The purpose of this circuit is to provide one switch power control (S_{37}) for the ELRPLL and for the Signal Generator Channel (S_{38}). The power from 3 of the 4 power supplies is connected such that the external sensing feature is used. The sense point is within the ELRPLL system. This decreases the voltage fluctuation at the ELRPLL due to contact resistance in J45 and S_{37}.

In general the critical components of the system that effect its response and transfer function are accurate to $\pm$ 3%. Therefore it is possible to specify the system transfer function to within $\pm$ 3%.

The level detectors are accurate to within $\pm$ 10 mv. For the level of signals considered this yields a level detecting accuracy of better than 1%.

The measurements of acquisition time are taken using 5 digits of timer accuracy. Therefore the accuracy of the measurement of acquisition time is limited by that of the ELRPLL transfer function plus that of the level detectors. Therefore it is conservative to specify the acquisition time accuracy as 5%.

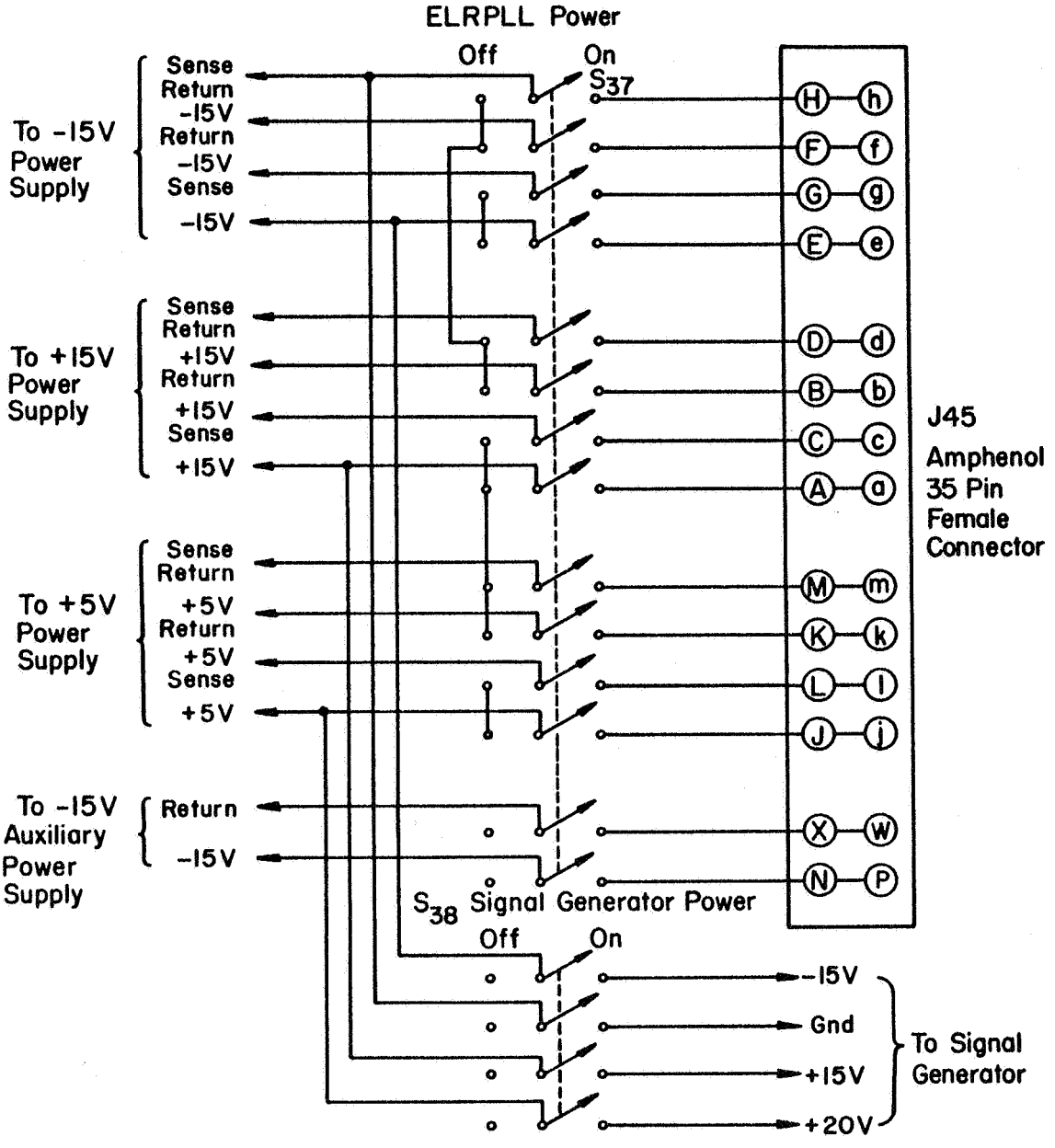


FIGURE B.15. ELRPLL, SIGNAL GENERATOR AND CHANNEL POWER DISTRIBUTOR.

APPENDIX C

EXPERIMENTAL SIGNAL GENERATOR AND CHANNEL

Appendix C is a detailed description of the Signal Generator and Channel. The circuit diagram of this system is presented and discussed. Its alignment procedure is explained.

Figure C.1 is the circuit diagram of the Signal Generator and Channel. The FM signal generator is a VCO very similar to the one used in the ELRPLL. The chief difference being that this one operates in the 95 - 105 KHz. band instead of its second harmonic. This VCO is located in the upper left hand corner of Figure C.1. It is an astable multivibrator with voltage frequency control. The frequency f_c is set by the Carrier Frequency Adjustment on the left. This is a 10 turn potentiometer on the front panel. The calibration is accomplished at two frequency points by P_1 and P_3.

J61 is the modulation input. The modulation level is controlled by the Modulation Step Attenuator. This attenuator has a range of 0 to 50 db in 10 db steps. The modulation level is controlled by S_{41} from the front panel. The level is calibrated by P_6. The VCO is temperature compensated by adjusting P_2.

The output of the VCO is isolated from the monitoring and output circuits by an emitter coupled current switch. The frequency of the VCO can be monitored at J60. The output voltage at J60 is limited to $\pm$ .6 V by back to back diodes. The signal at the other side of the current

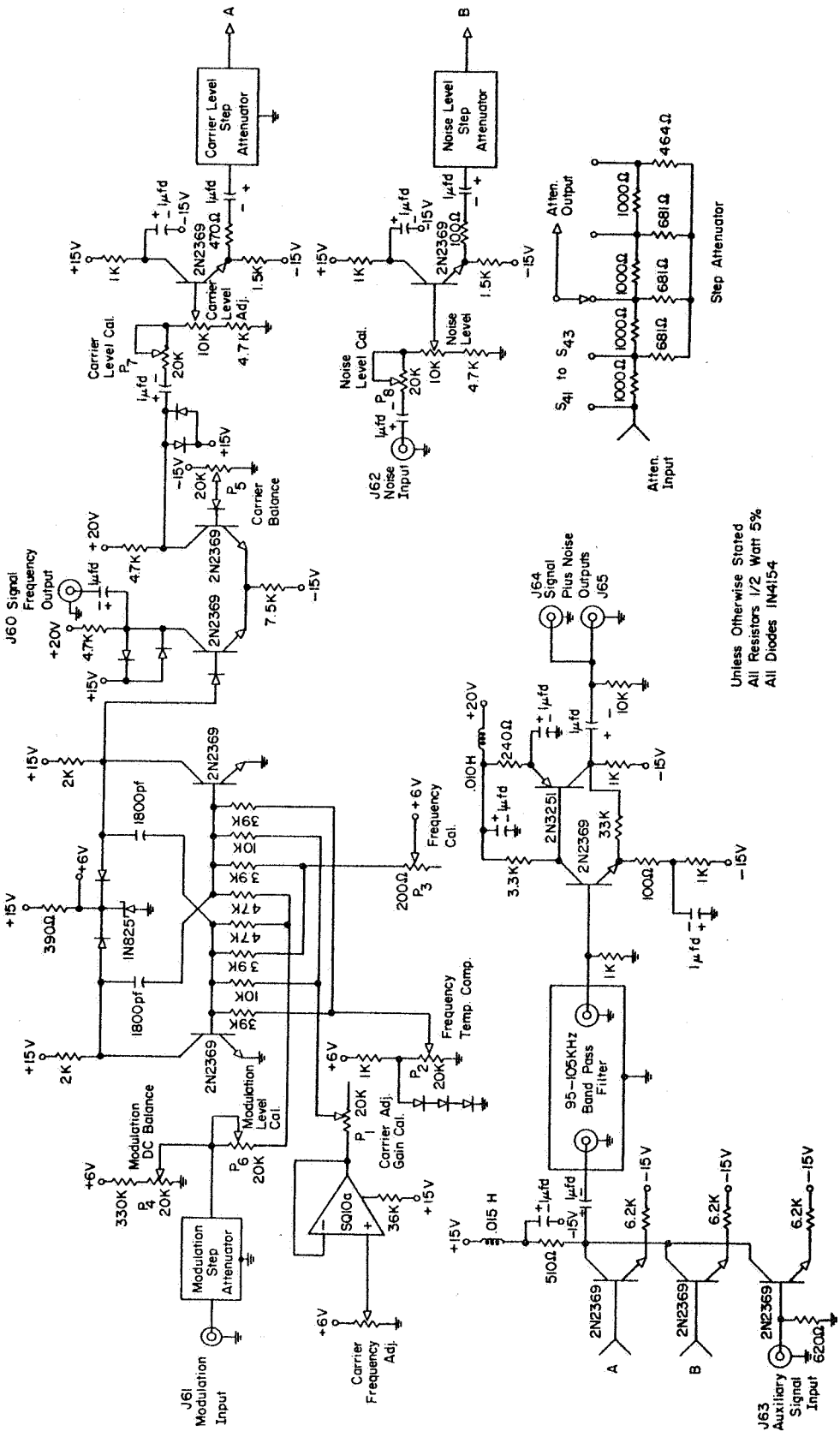


FIGURE C.1. SIGNAL GENERATOR AND CHANNEL.

switch is also limited by diodes. P_5 is used to adjust the symmetry of the signal at P_7. P_7 is used for calibrating the carrier level. The level of the calibrated carrier is controlled by the Carrier Level Step Attenuator in 10 db steps and continuously over a 10 db range by the Carrier Level Adjustment. Both of these adjustments are located on the front panel.

The signal from a GR 1309B generator is input at J62. The level of it is calibrated by P_8. The level of the calibrated noise is controlled by the Noise Level Step Attenuator in 10 db steps and continuously over a 10 db range by the Noise Level Adjustment. Both of these adjustments are located on the front panel.

The noise and modulated carrier are summed with the Auxiliary Signal Input and the result is filtered by the 95 - 105 KHz. Band Pass Filter. The measured transfer function of this filter is shown in Figure C.2. It has a seven pole butterworth bandpass response. The ripple was found to be less than .3 db peak to peak. This filter is used to simulate the bandpass of the receiver that normally preceeds a PLL. The output of the filter is amplified and the resulting signal plus noise is available at J64 and J65.

The specifications on the Signal Generator and Channel are:

I. FM Signal Generator

A. The Carrier

1. The residual FM, is less than 1 Hz. for $f_m > 1$ Hz.

2. The power supply effect on frequency is less than 10 Hz./volt.

3. The frequency range is 95 - 105 KHz.

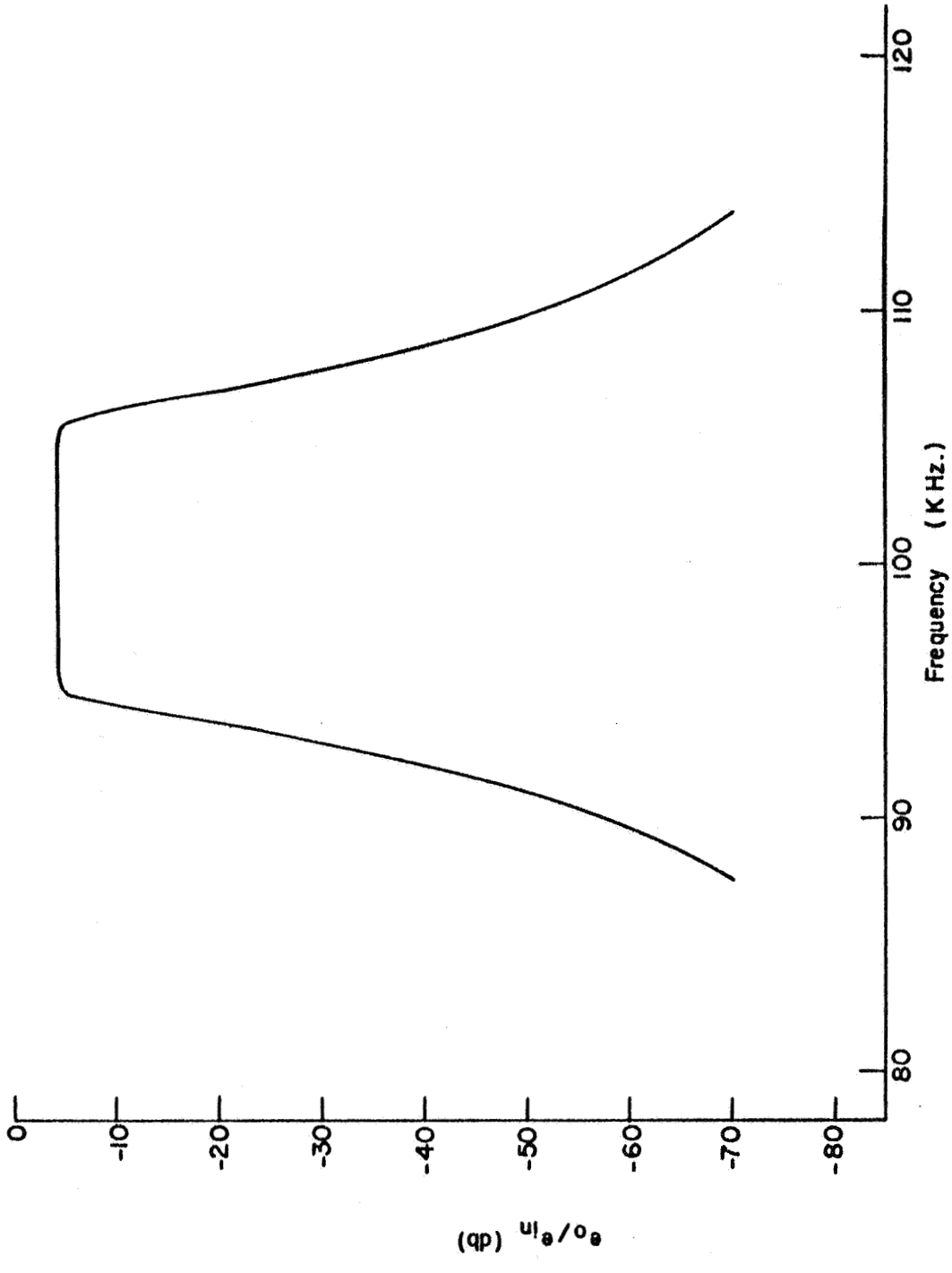


FIGURE C.2 CHANNEL FILTER FREQUENCY RESPONSE

4. The long term stability is 30 Hz./day after 1 day operation in a temperature stabilized room.

B. The Modulation

1. The maximum deviation is 95 to 105 KHz.

2. The maximum bandwidth is DC to 5 KHz.

3. The attenuator range is continuous 0 - 60 db.

II. The Channel

1. The input noise spectrum must be flat to 105 KHz.

2. The output noise spectrum is flat $\pm$ .14 db over 96 - 104 KHz.

3. The S/N range is continuous from - 60 to 60 db in 10 KHz. bandwidth.

4. The 3 db channel bandwidth is less than 12 KHz. and greater than 10 KHz.

5. The channel attenuation below 89 KHz. and above 112 KHz. is greater than 60 db with respect to that in its pass band.

Appendix D

ACQUISITION TIME EXPERIMENT

Appendix D is a detailed description of the ELRPLL acquisition time test fixture. The circuit diagrams of this system are presented and discussed.

The purpose of this test fixture is to facilitate the measurement of the acquisition time. It makes it possible to make measurements either individually or in rapid succession automatically.

The system has two parts. Section D.1 deals with the Level Detector. Section D.2 deals with the ELRPLL Control System and discusses the various modes of operation.

D.1. The Level Detector

Figure D.1 is the circuit diagram of the Level Detector. The system has 6 of these. This circuit tests the voltage of the signal at one of J33 through J38 against one or two thresholds and generates a binary signal based on one of several possible logical relations. This depends on the position of one of S_{18} through S_{23}. If the switch is down the output at pin 9 is negative if the input is less than a preset threshold. The threshold is set by the Level Set control. If the switch is in the center position, it tests if the voltage is between two thresholds. The width of the acceptance region is set by one of S_{12} through S_{17} to the voltage width desired. If one of S_{18} through S_{23} is put in the up position then

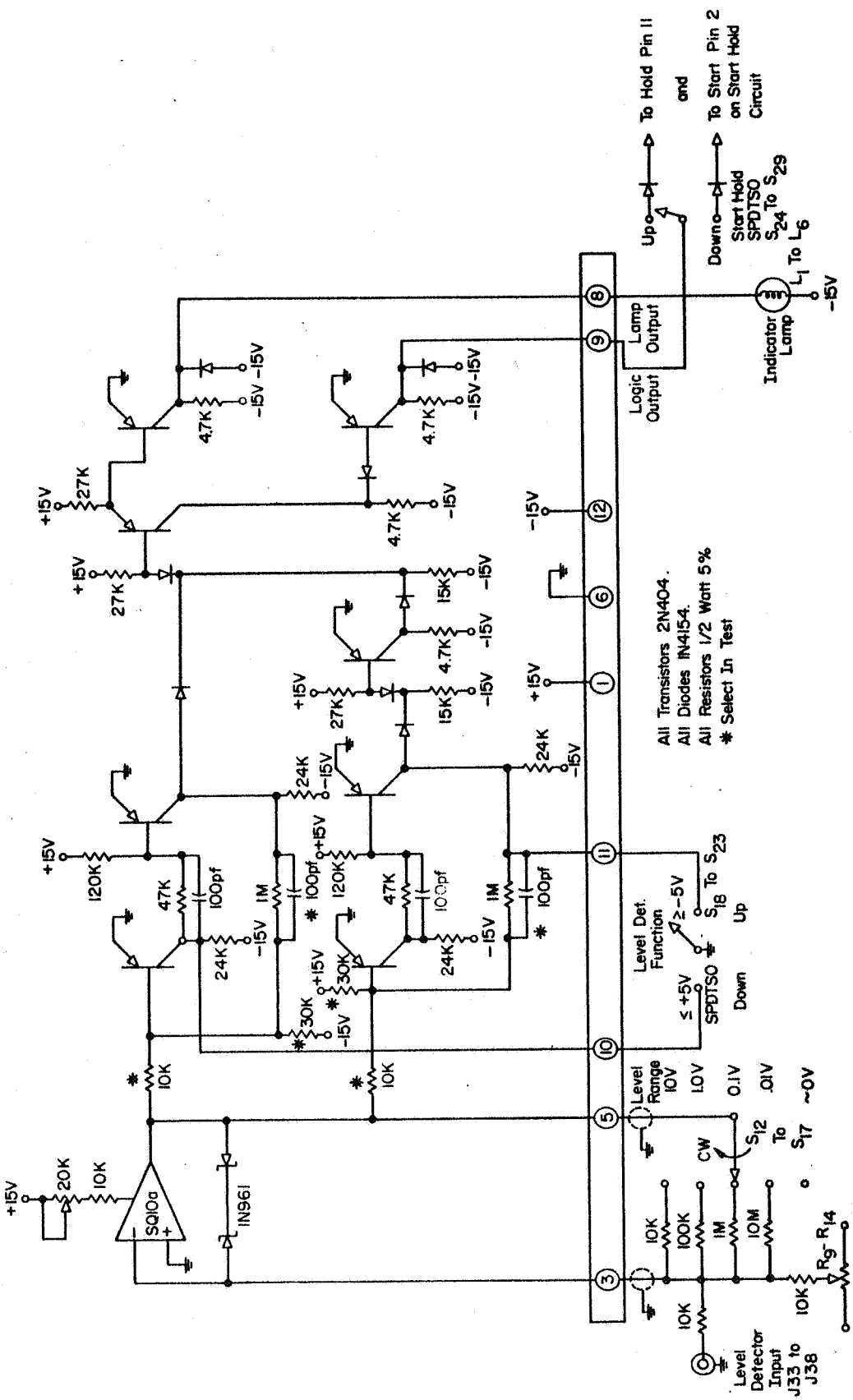


FIGURE D.I. LEVEL DETECTOR.

it tests if the voltage is greater than a preset threshold.

When the comparison is true, one of the lamps L_1 through L_6 is lit and either a start or hold logic signal is anded with the other Level Detector logic signals depending on the positions of S_{24} through S_{29}.

The width of the region of comparison is changed by changing the gain of the operational amplifier. When its output passes 5 V the upper bistable circuit switches state. If the amplifier output passes - 5 V the lower bistable circuit switches state.

A logic circuit selected by one of S_{18} through S_{23} generates the logic signal output at pin 9 and the lamp output at pin 8.

D.2. The ELRPLL Control System

Figure D.2 is the circuit diagram of the ELRPLL Control System. The purpose of this system is to sense when the initial and final conditions of the ELRPLL are within some prescribed space and generate control signals to start and/or hold the ELRPLL. They are used to control a timer so that the elapsed time of a loop event may be determined.

When the intersection is true of the logical signal from J39, the start inputs from LD_1 through LD_6, the switch (S_{35}) is not up, the hold output is not actuated and S_{34} is in the center position, then the start flip-flop is set in a start position. When this occurs the Initial Condition Controllers are disconnected from the loop filter. The lamp L_7 is extinguished and a positive going pulse appears at J41. This can be used to start a timer.

When the intersection is true of the logical signal from J40, the hold inputs from LD_1 through LD_6, the switch (S_{36}) is in the center position and the start output is not actuated, then the hold flip-flop is

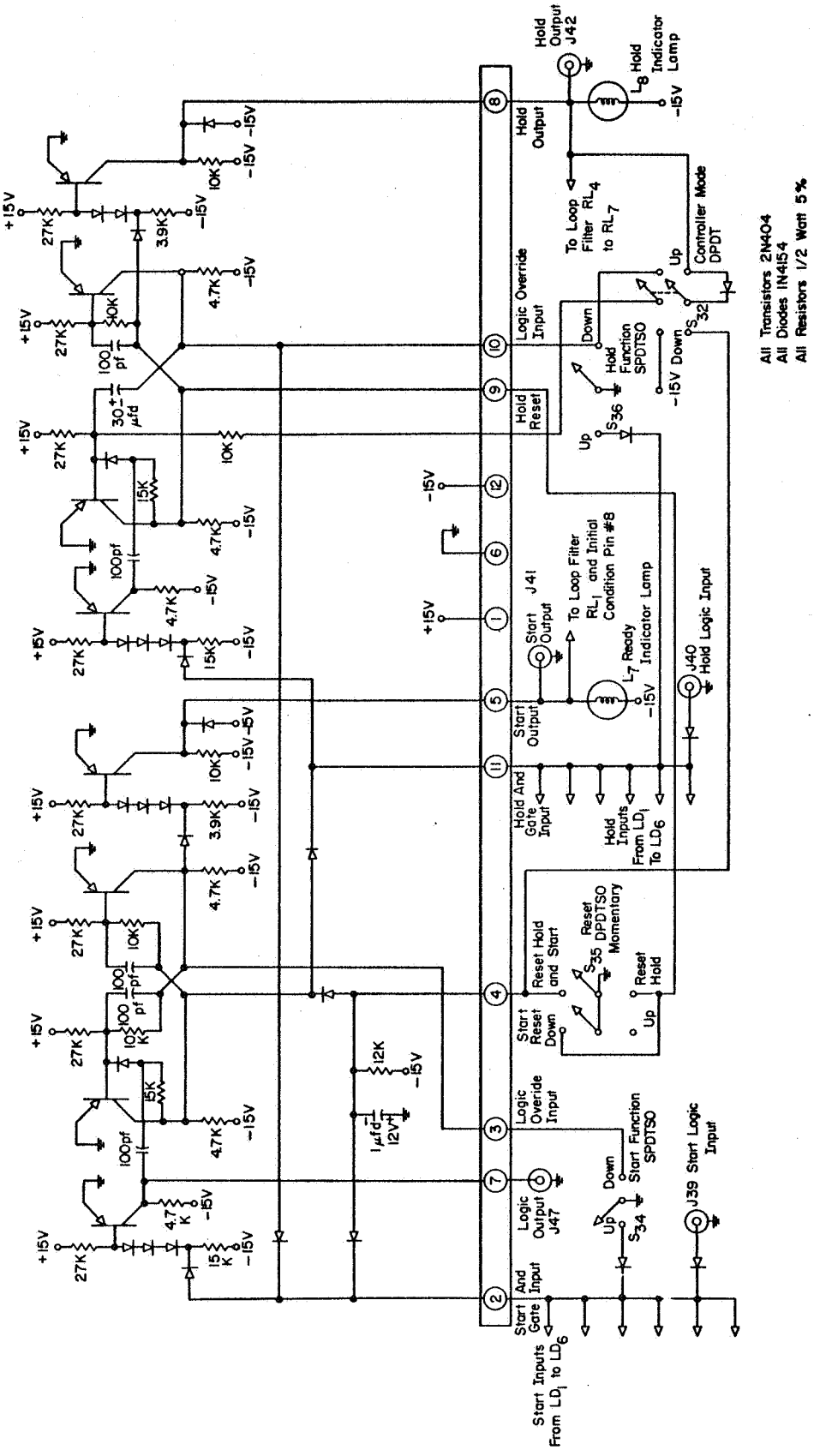


FIGURE D.2. ELRPLL CONTROL SYSTEM.

actuated, the lamp L_8 is lit and a hold pulse is generated at J42. When S_{32} is up the system does not automatically reset and will remain indefinitely in the hold condition until manually reset by S_{35}. If S_{32} is down the system functions in an automatic mode and resets itself after being in the hold state for 1 second. In this case the right flip-flop is connected in a monostable configuration and resets itself. At the same time the left flip-flop is reset which actuates the Initial Condition Controllers so that the loop filter initial conditions are reset for another event. As soon as the resetting is complete, the start coincidence logic is able to test for the start condition. This process repeats itself until S_{32} is switched up.

It is possible to manually start or hold the ELRPLL by switching down S_{34} or S_{36} respectively. It is also possible to inhibit the start or hold operation by switching to the up position S_{34} or S_{36} respectively.

It is possible to reset the hold circuit by pushing S_{35} up. It is possible to reset the hold and the start circuits by pushing S_{35} down.

Using this system it is also possible to get an estimate of the joint distribution function of a set of loop variables.

APPENDIX E

FM THRESHOLD EXPERIMENT

Appendix E contains a description of the experimental procedure used to determine the FM threshold of the ELRPLL and of the Threshold Text Fixture.

The procedure requires the measurement of the I/O S/N in the output bandwidth for the ELRPLL. This is done for a class of ELRPLL and signal parameter values. The Threshold Test Fixture shown in Figure E.2 is used to facilitate the measurement of the output S/N level. This circuit is used in connection with the auxiliary amplifiers in Figure E.3, a Philbrick analog multiplier, LPF, and a digital voltmeter in the measurement set up shown in Figure E.1.

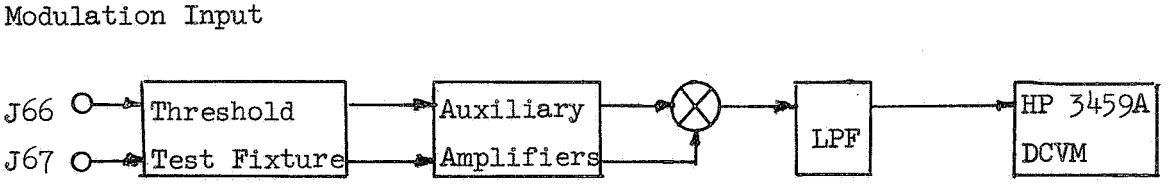


Figure E.1. Threshold Test Set Up Detail

S_{40} controls the mode of measurement. When S_{40} is in position 1 the digital DCVM reading is proportional to the RMS output signal voltage.

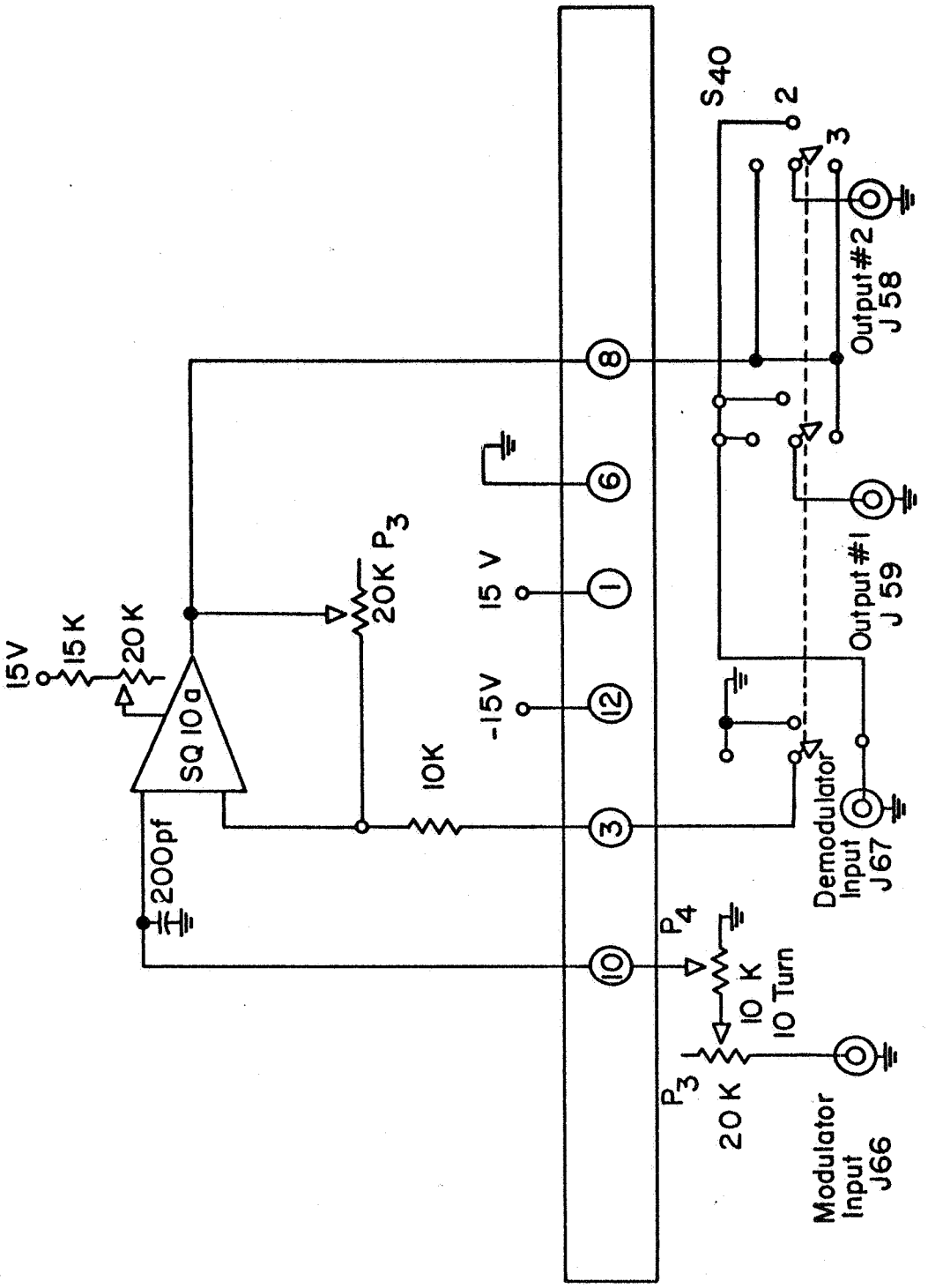


FIGURE E.2. THRESHOLD TEST FIXTURE

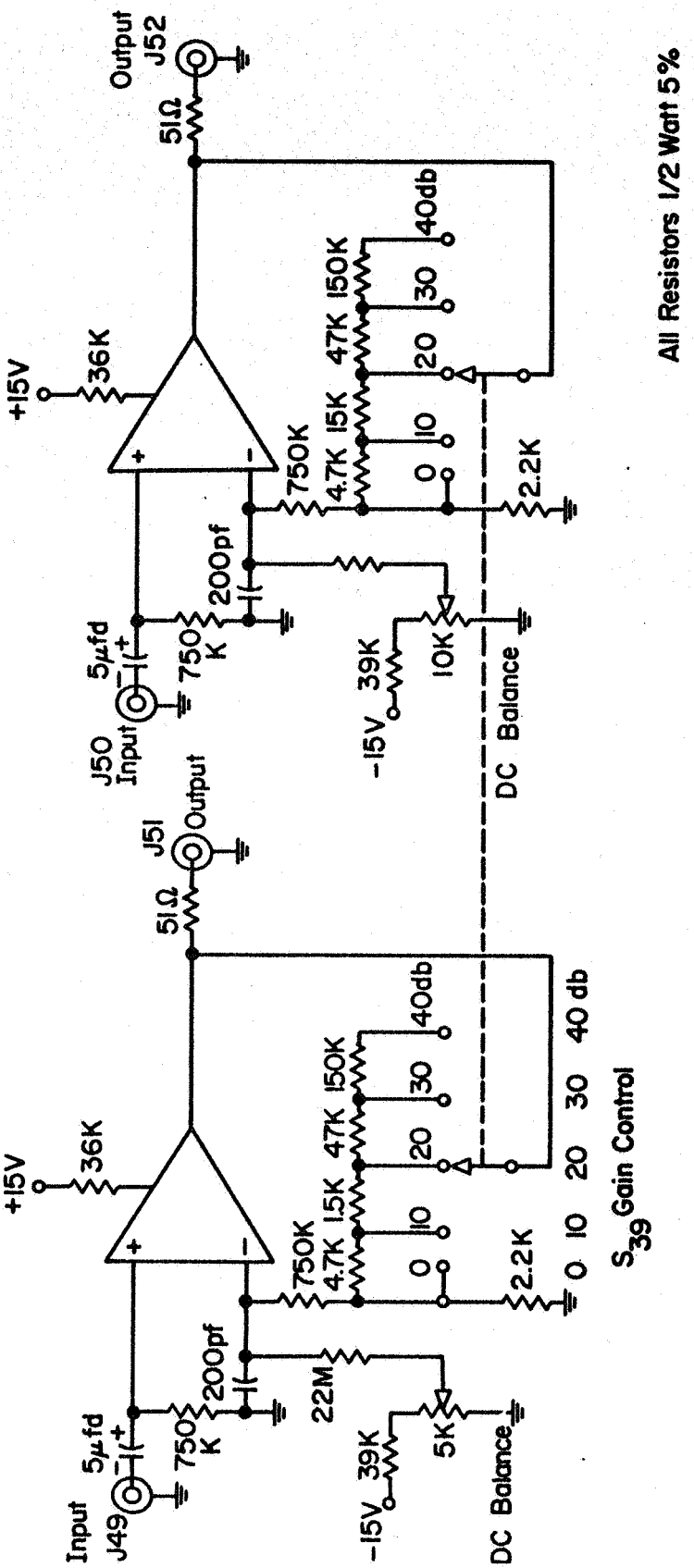


FIGURE E.3. AUXILIARY AMPLIFIERS.

When it is in position 2 the reading is proportional to the output signal plus noise power. When it is in position 3 the reading is proportional to the output noise power.

In measuring the output S/N, first the ELRPLL system parameters are set. Then the signal parameters are set beginning with the no noise case. With S_{40} in position 3 and P_4 in its clockwise position, P_3 is adjusted for minimum reading of the voltmeter. The switch is set to position 1 and the auxiliary amplifier and LPF attenuators are set so that the meter reading is - .1.

When the normalization procedure is completed the input S/N is set to the first desired level. This is usually the maximum S/N that yields a measurable reading of the output noise on the meter. Then the output signal voltage is read using switch position 1. The output signal power is 100 times the square of this reading. Switching to position 2, the output signal plus noise power is 10 times the meter reading. P_4 is set to 100 times the signal voltage reading and the switch is set to position 3. The noise power is 10 times the meter reading. The ELRPLL and signal parameter values and the output signal, signal plus noise and noise powers are punched on IBM cards. These are computer processed to correct the data for known measurement biases. This process is repeated for each value of input S/N level. Then a new set of system parameters is selected and the initial normalization must be repeated.

The measurement corrections mentioned include the following: 1. the data is corrected for changes in the meter loading effect that occur when changing scales or LPF time constants; 2. the input S/N in the output band is calculated from that in the input band; 3. the output noise is

corrected by calculating a weighted sum of the measured noise and the noise calculated from the difference of the signal plus noise power and the signal power, where the weighting is the inverse of the variance of the measurements; 4. the output signal is corrected by a factor of 2 due to the fact that the ELRPLL output base band filter has a 3 db cutoff frequency equal to that of the sinusoidal modulation; 5. the output noise power is corrected by a factor depending upon the ratio of the ELRPLL output filter equivalent noise to 3 db bandwidths so that the output noise is referred to the 3 db bandwidth; 6. the output S/N in the output band is calculated from the corrected signal and noise powers.

A total of 1200 sets of data points for I/O S/N levels were obtained. These are plotted by the Calcomp Plotter in Figures 6.2 to 6.19 and 6.21 to 6.27.

The outputs of the Threshold Test Fixture are amplified by the auxiliary amplifiers. The gain of these is adjustable in 10 db steps by S_{39}. This increases the dynamic range of the measuring system.

The auxiliary amplifiers' outputs are multiplied by the Philbrick multiplier. The multiplier output is low pass filtered. The time constant of this LPF has two settings. These are 4 seconds and 40 seconds. The latter is necessary for the case of random modulation and the former is sufficient for most cases of sinusoidal modulation. Provision is made to make a fine adjustment in the output level to aid in normalizing the output signal power for the no input noise case.

APPENDIX F

RANDOM MODULATION GENERATOR

Appendix F is a description of the Random Modulation Generator. Figure F.1 is the circuit diagram of this device. It consists of a pair of LPF amplifiers, a mixer driver and a mixer.

The amplifier on the left has a LPF with a cutoff frequency of 1.9 KHz. It filters and amplifies the random signal from the noise generator. The level of the filtered noise is adjusted by an HP 350D attenuator.

The attenuated signal is mixed by a 1 KHz. gating signal from the mixer driver, the 2N1613. The frequency translated result is further filtered and amplified to a maximum RMS level of 3 V. The spectrum of the noise is shaped to the desired modulation spectrum by the Spectrum Analog Filter.

The only alignment is the balancing of the two operational amplifiers with the potentiometers.

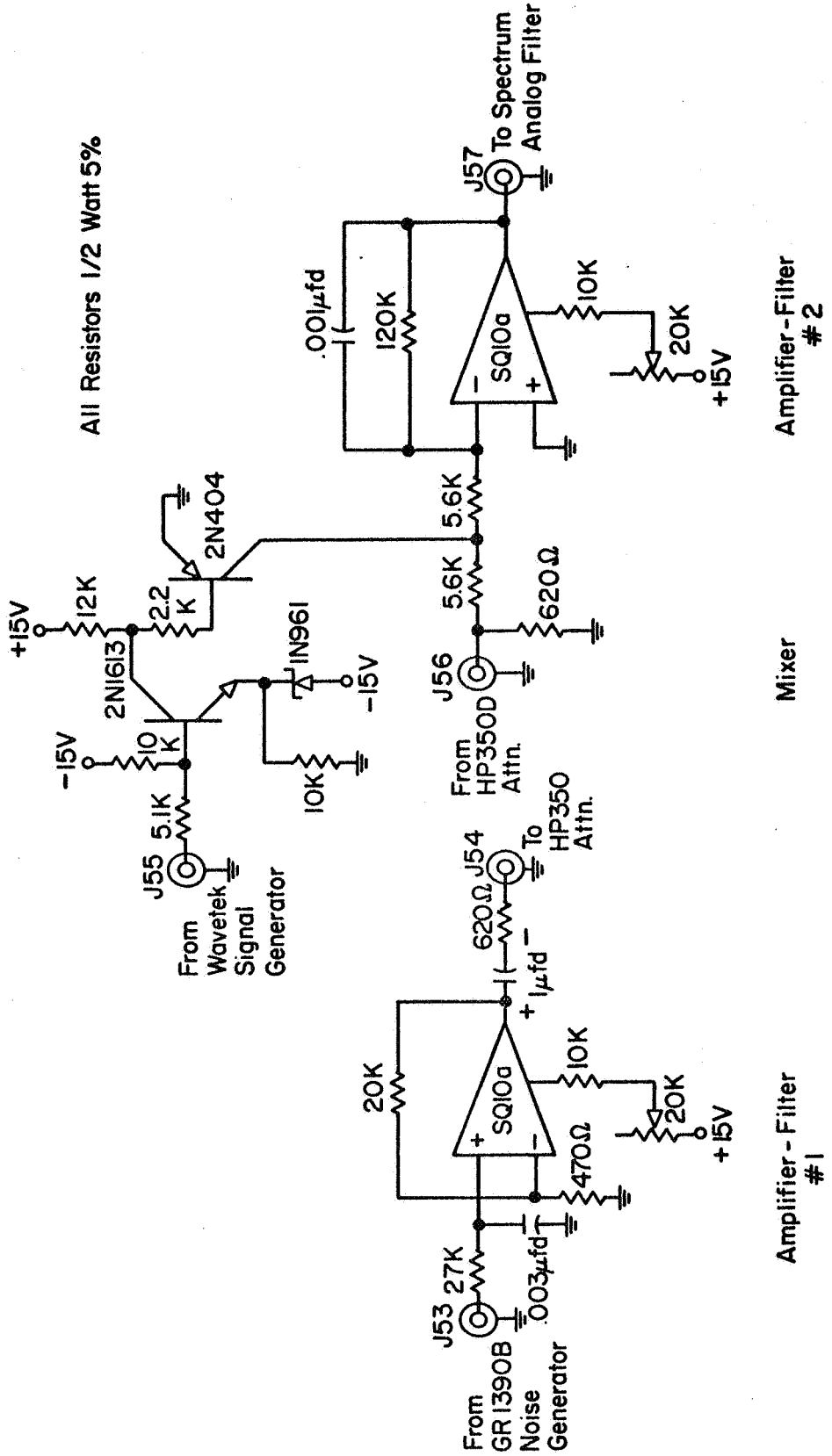


FIGURE F.1. RANDOM MODULATION GENERATOR.